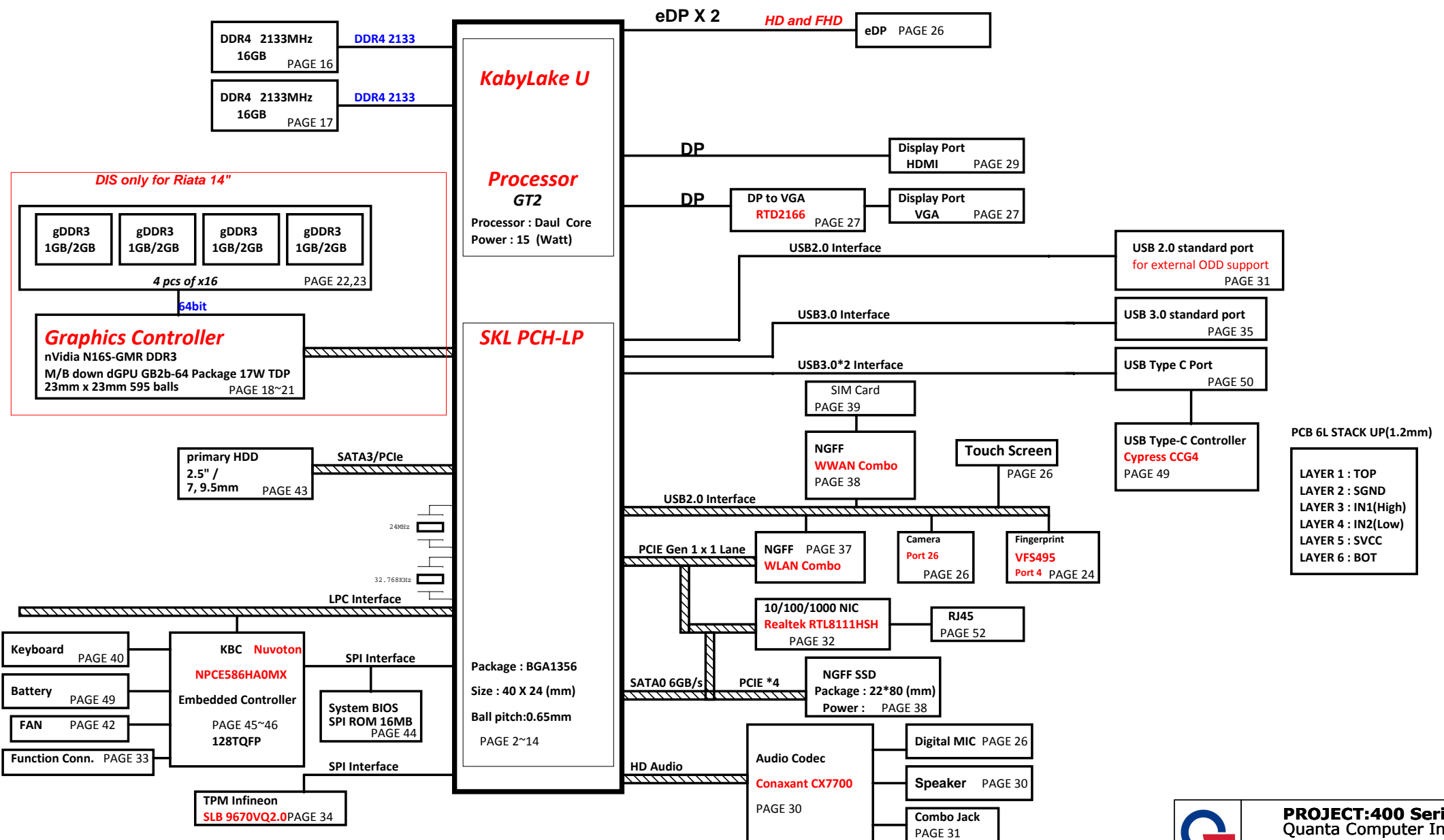
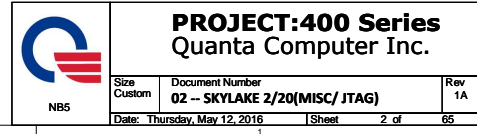
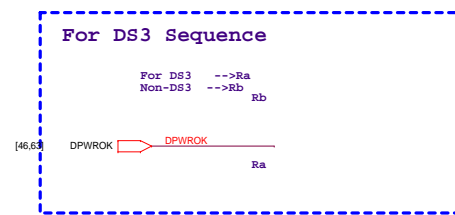
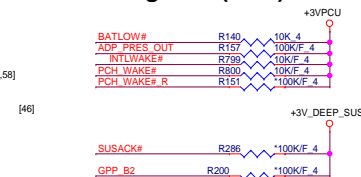
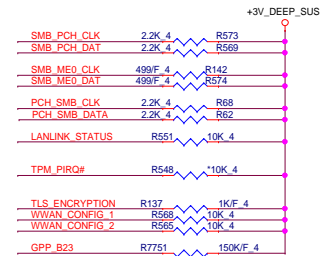


Reilly 13"/Rourke 14" KabyLake -U (UMA/DIS) Schematics01

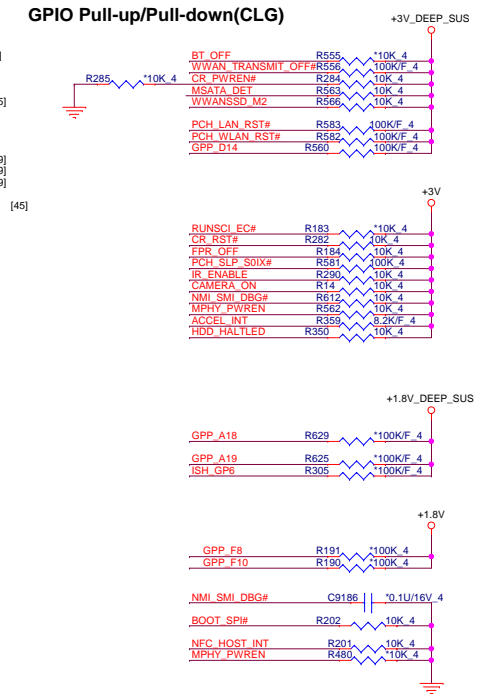
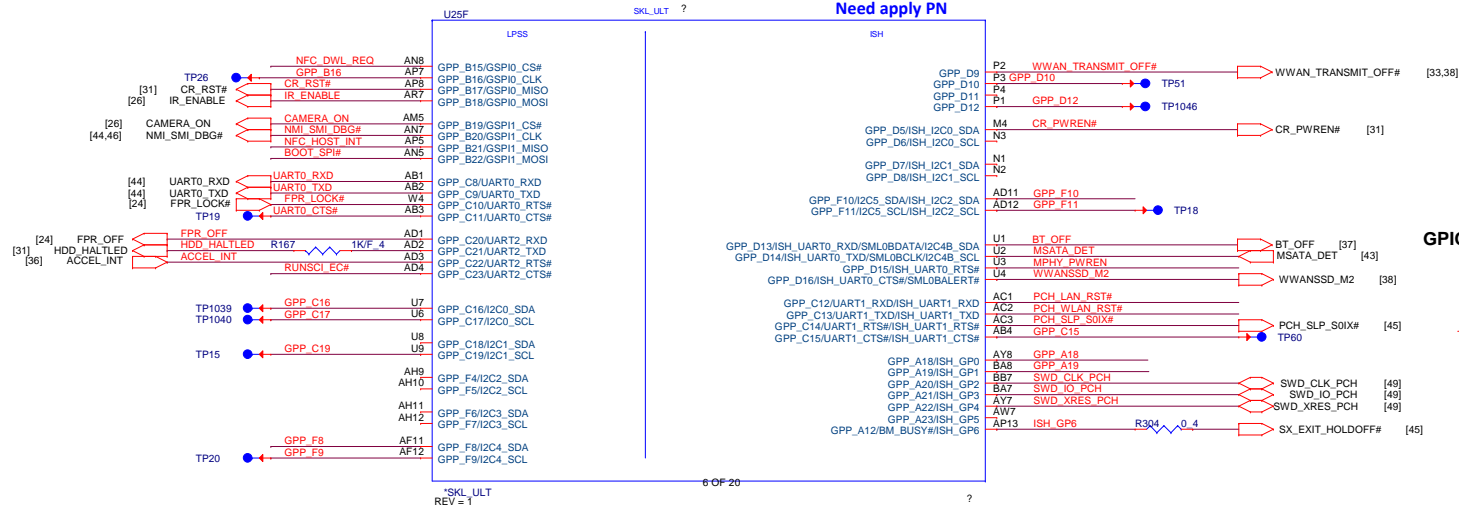






PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 03 – SKYLAKE (SPI/LPC/SMB/PM)	Rev 1A
Date: Thursday, May 12, 2016	Sheet 3 of	65



Codec table		
	CX7700	CX7501
R206	INSTAL	UNINSTAL
R207	UNINSTAL	INSTAL

[2,3,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]



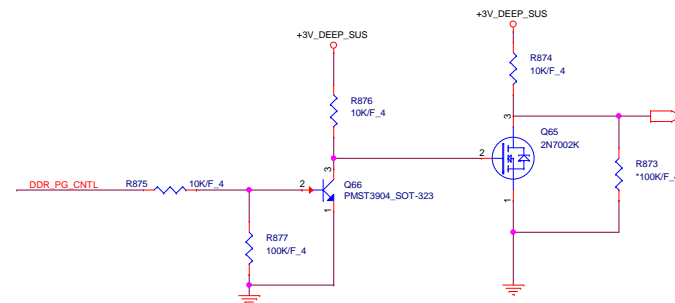
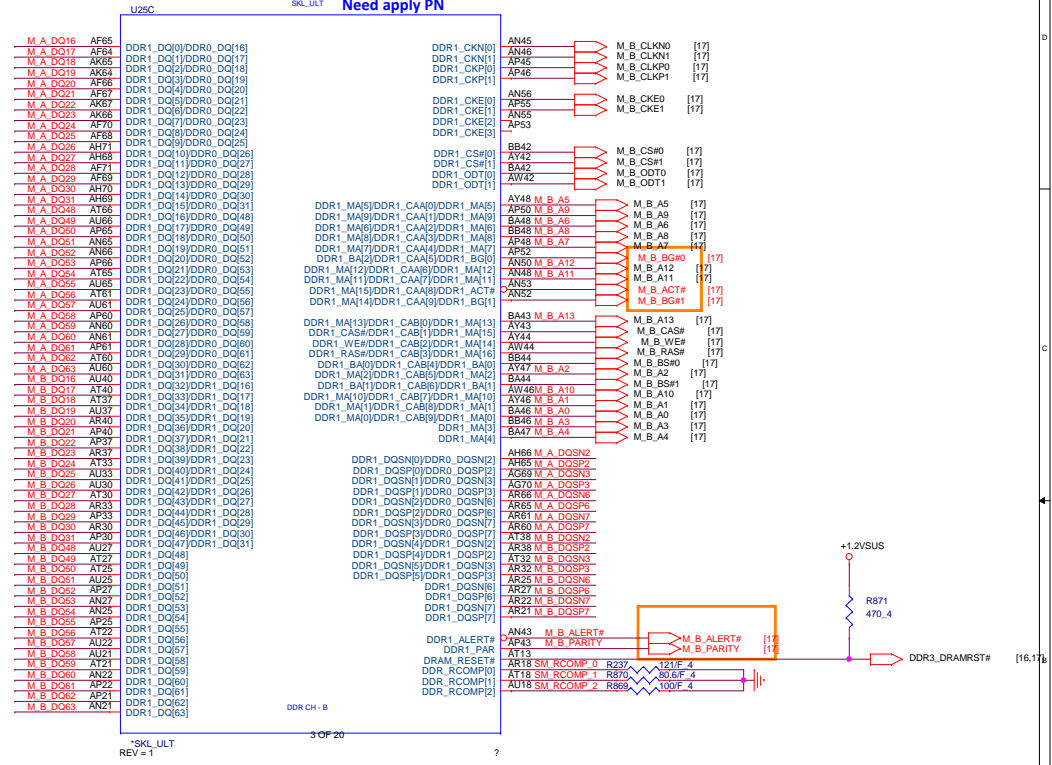
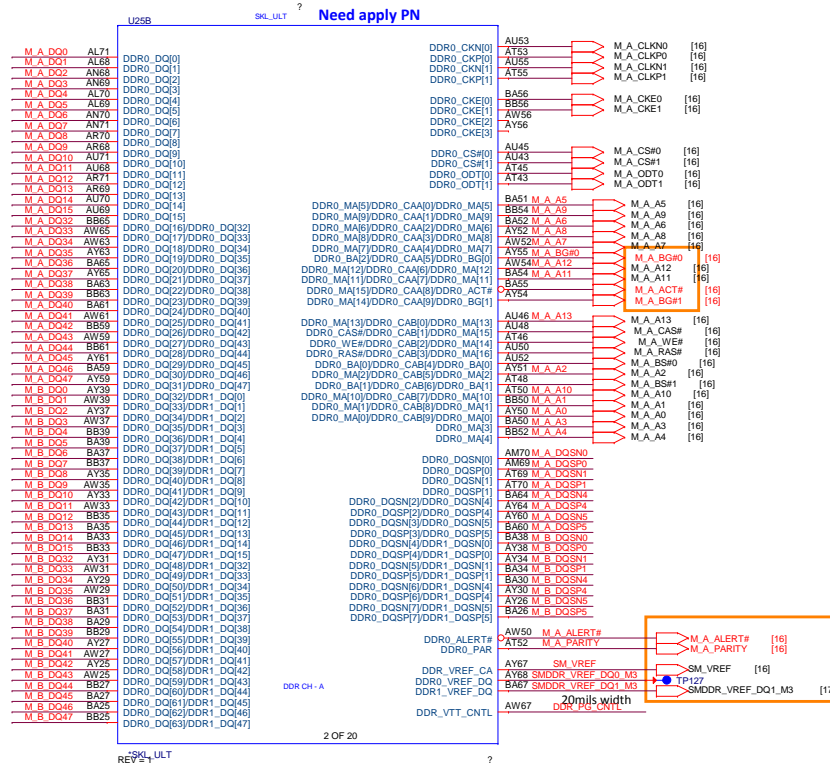
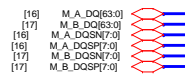
PROJECT:400 Series
Quanta Computer Inc.


Size Custom	Document Number 04 -- SKYLAKE (GPIO)	Rev 1A
Date: Thursday, May 12, 2016	Sheet 4 of	65

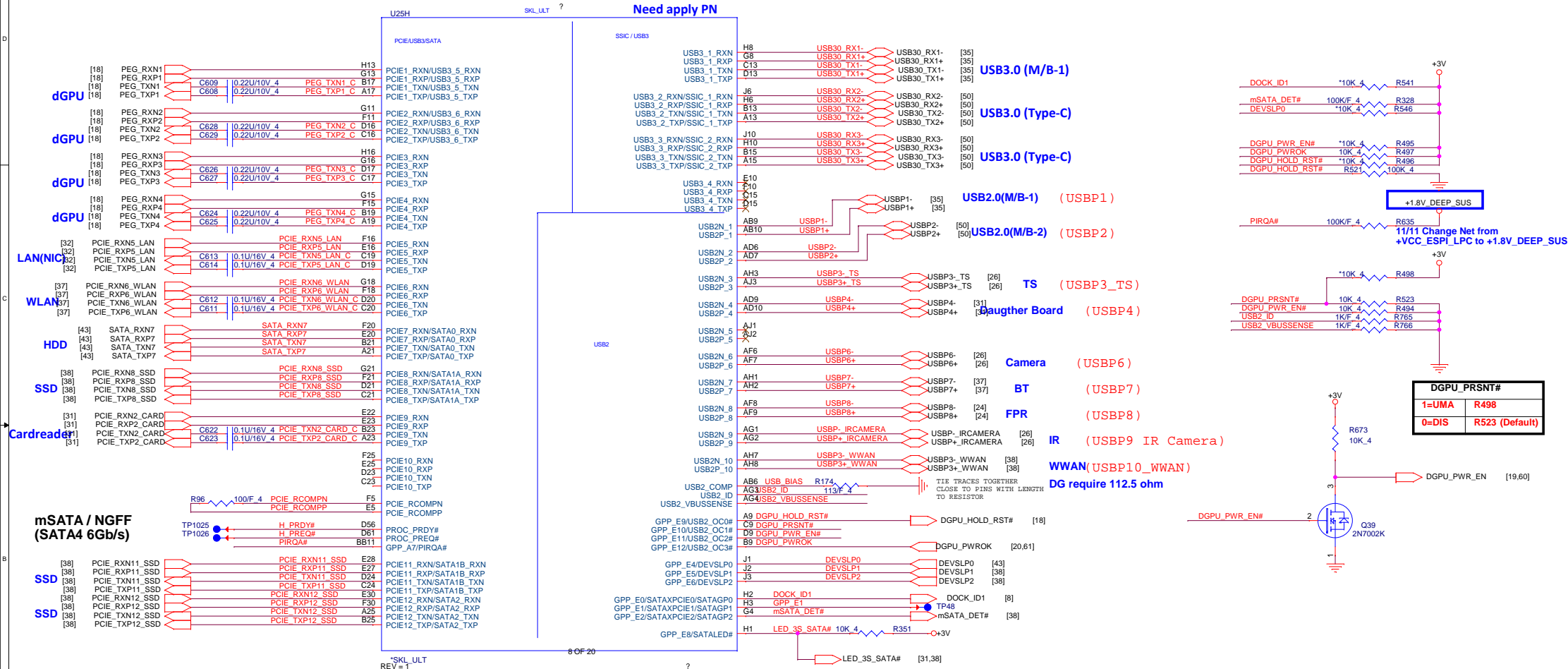
[illegible]UNINSTAI

I'm from VIETNAM **sualaptop365**


SkyLake ULT Processor (DDR4)



 NBS	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 06 – SKYLAKE (DDR3-A/B I/F)	Rev 1A
Date: Thursday, May 12, 2016		Sheet 6 of 65	

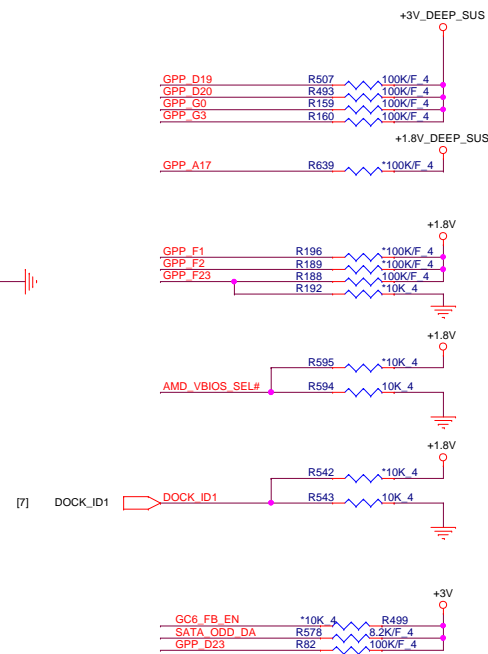


[2,3,4,5,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]
[3,4,5,6,8,10,28,37,44,45,47,55,58,63]



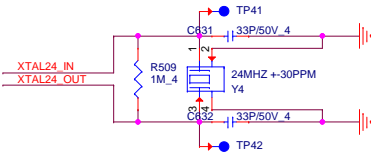
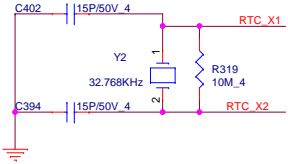
PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 07 - SKYLAK (PCIE/USB)	Rev 1A
Date: Thursday, May 12, 2016		Sheet 7 of 65

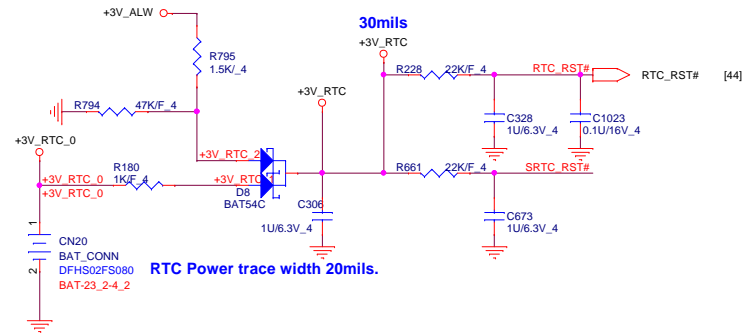


AMD_VBIOS_SEL#	DOCK_ID1
00= VBIOS 1	
01 = VBIOS 2 (Reserve for new die)	
10 = VBIOS 3 (Reserve for new die)	
11=UMA	R595,R542

RTC Clock 32.768KHz

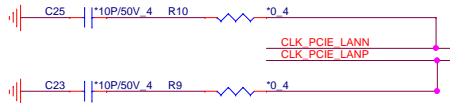
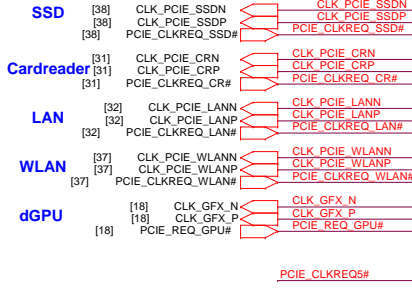


RTC Circuitry(RTC)

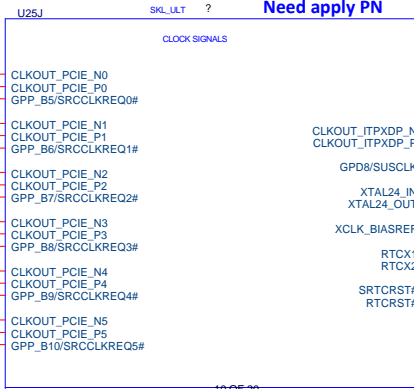


RTC Power trace width 20mils.

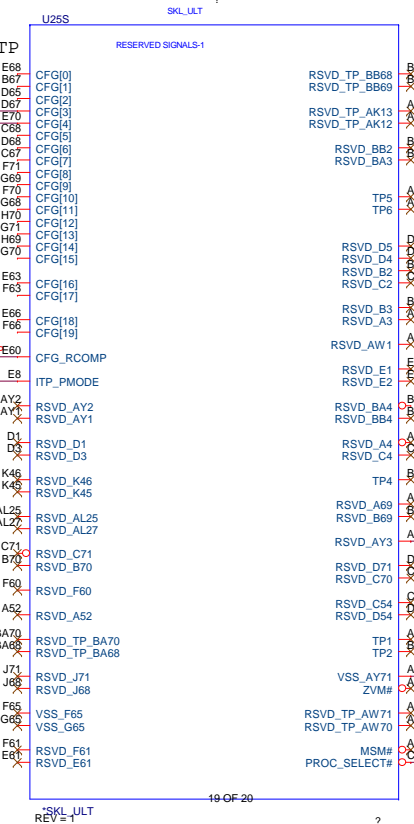
+VCCSFR [2,3,11,13,45]
+1.0V_DEEP_SUS [10,54,55,58]
+3V [2,3,4,5,7,8,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]



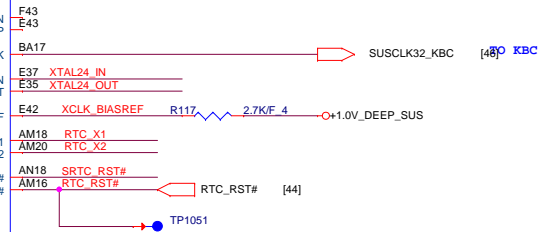
CFG0-19 need Reserve TP



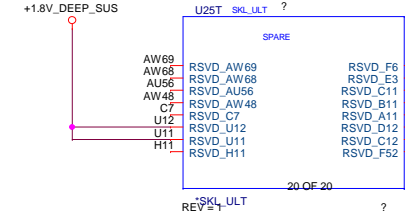
*SKL_ULT REV=1




*SKL_ULT REV=1



CLK_REQ/Strap Pin(CLG)



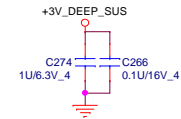
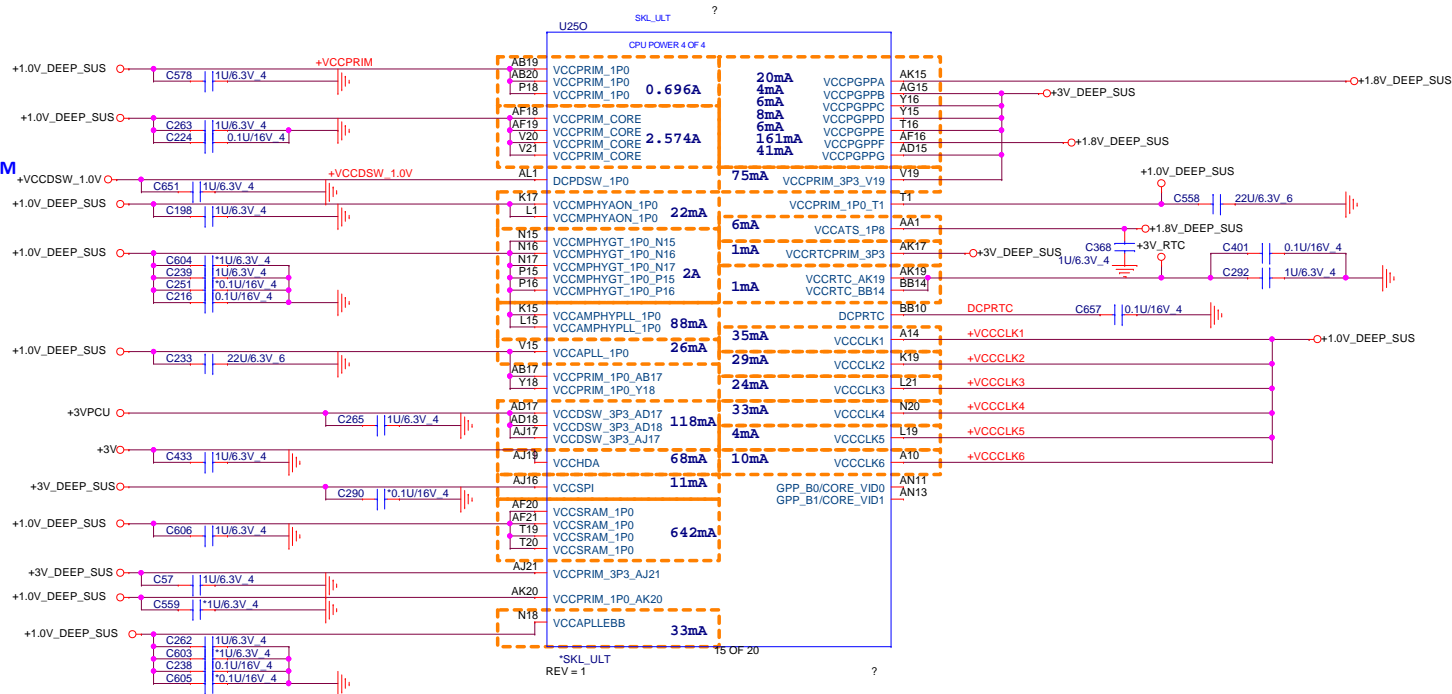
*SKL_ULT REV=1



PROJECT:400 Series
Quanta Computer Inc.

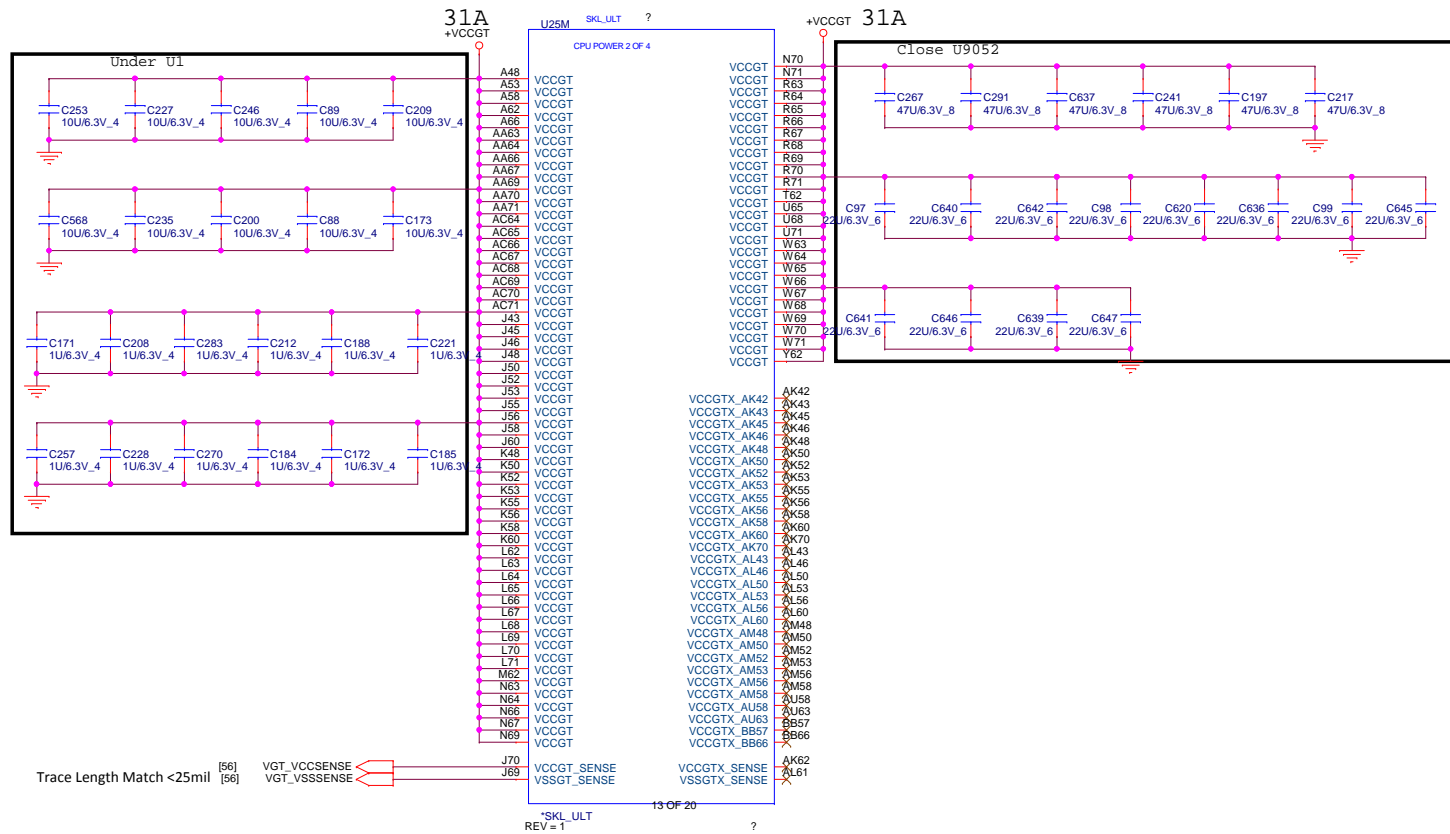
Size Custom	Document Number 09 - SKYLAKE (CLK/RSV/RTC)	Rev 1A
Date: Thursday, May 12, 2016	Sheet	9 of 65

PCH Internal VRM

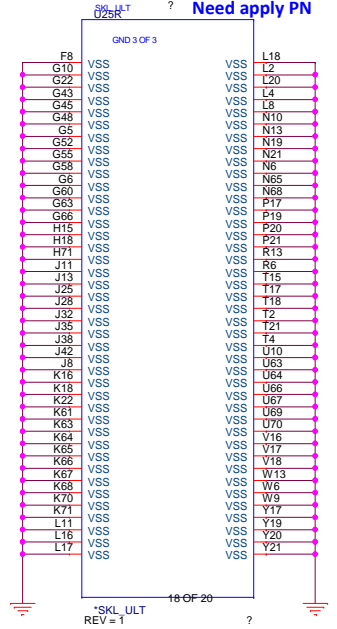
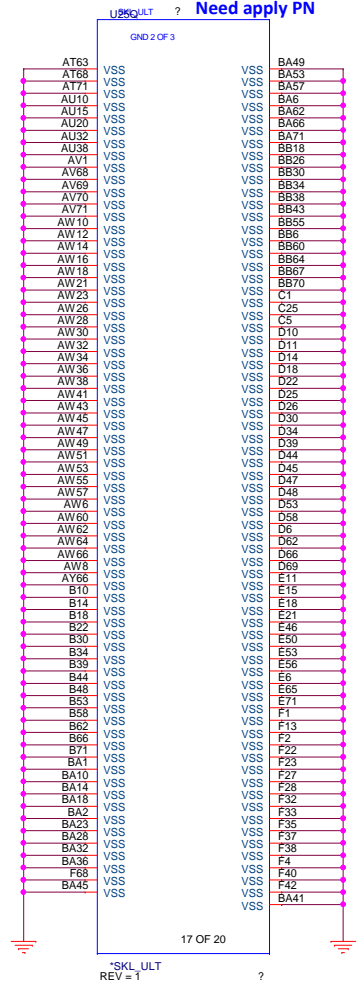
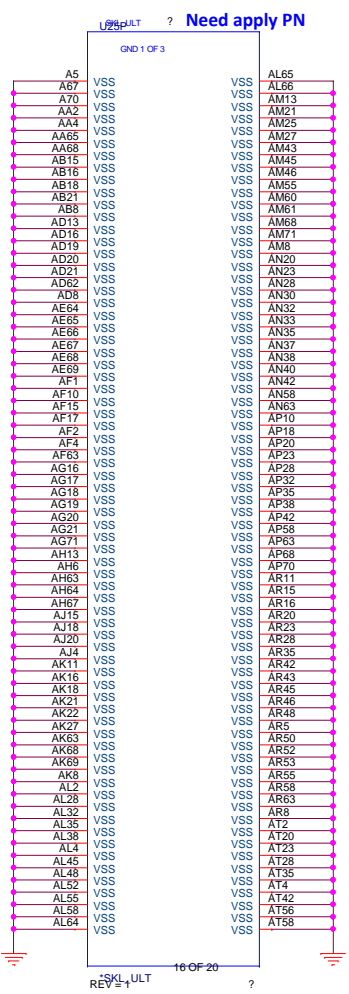


+3V_DEEP_SUS	[3,4,5,6,8,28,37,44,45,47,55,58,63]
+3VPCU	[3,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63]
+1.0V_DEEP_SUS	[9,54,55,58]
+VCC_PRIM	
+3V	[2,3,4,5,7,8,9,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]
+1.8V_DEEP_SUS	[3,4,7,8,9,45,54,63]

	PROJECT:400 Series		
	Quanta Computer Inc.		
	Size Custom	Document Number 10 - SKYLAKE (PCH POWER)	Rev 1A
	Date: Thursday, May 12, 2016	Sheet 10 of	65



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



D

D

C


C

B

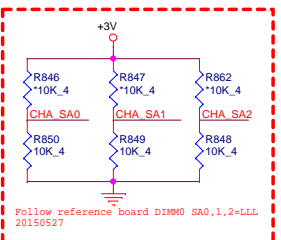
B

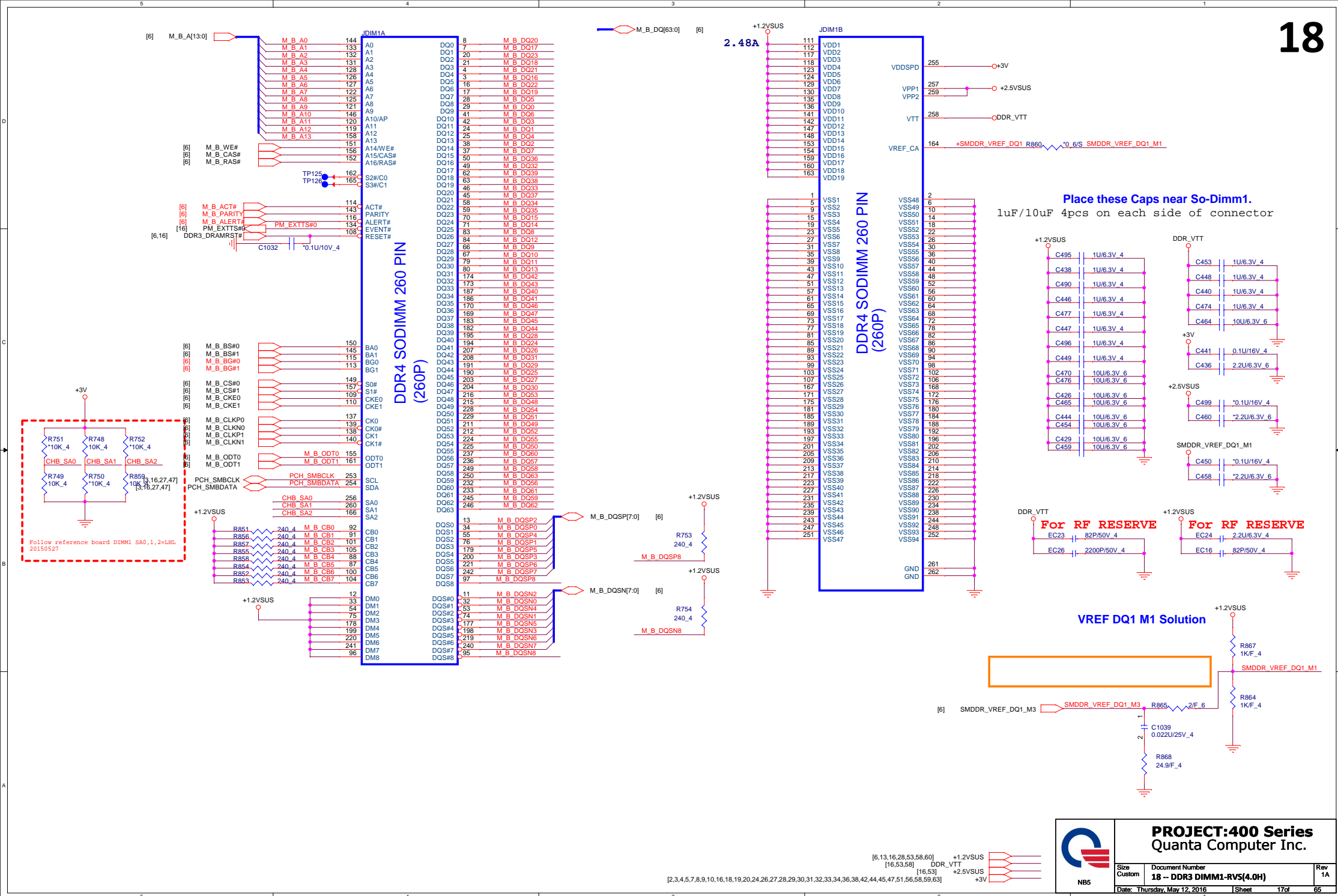
A

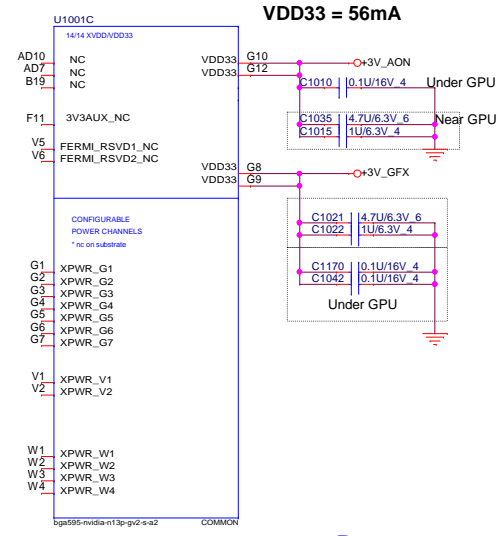
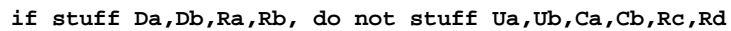
A

	PROJECT:400 Series Quanta Computer Inc.		
	Size	Document Number	Rev
	15 -- HSW XDP & APS		1A
Date: Thursday, May 12, 2016		Sheet	15 of 65

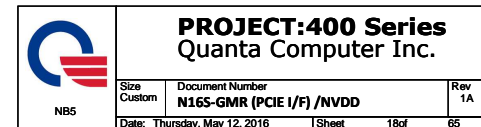
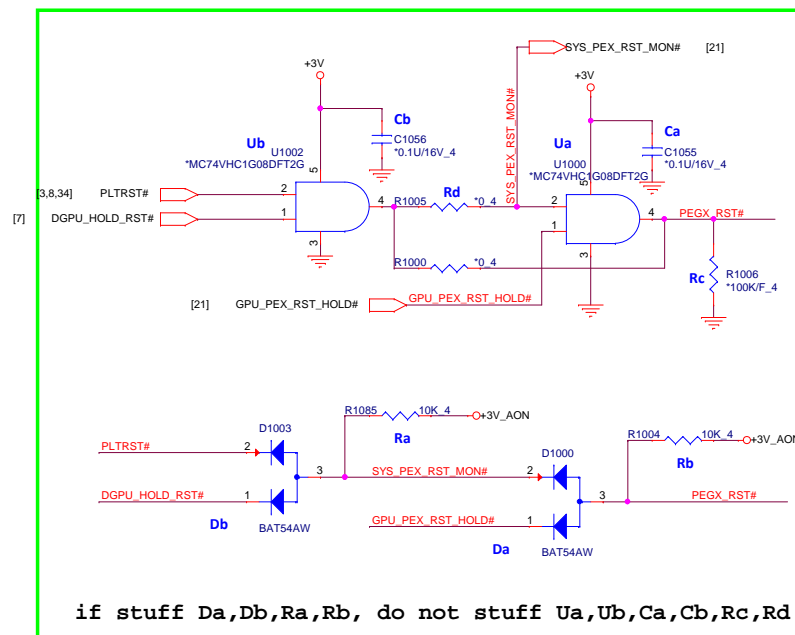
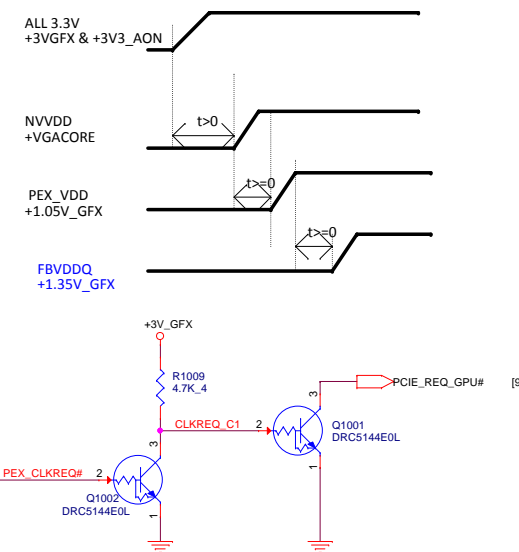
I'm from VIETNAM [sualaptop365](#)



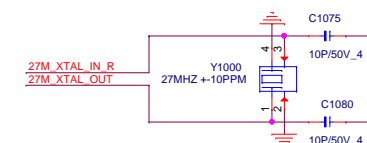
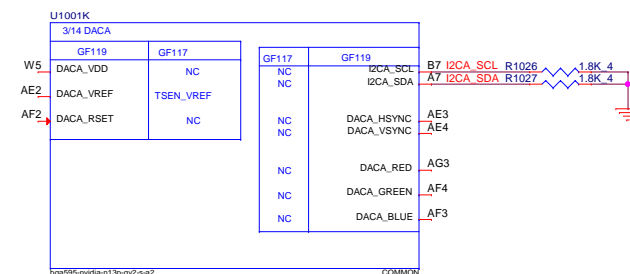
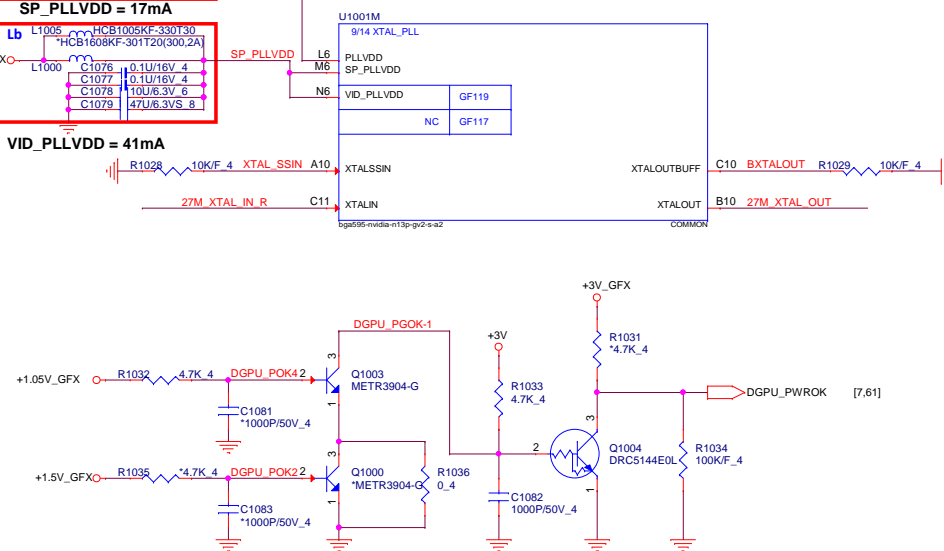
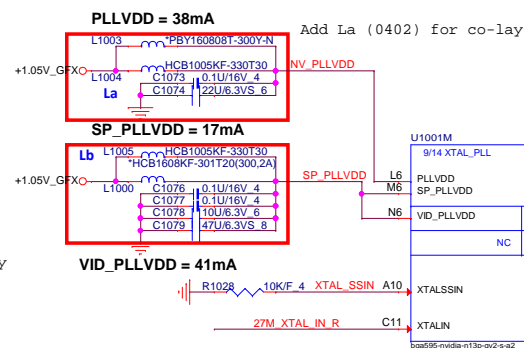
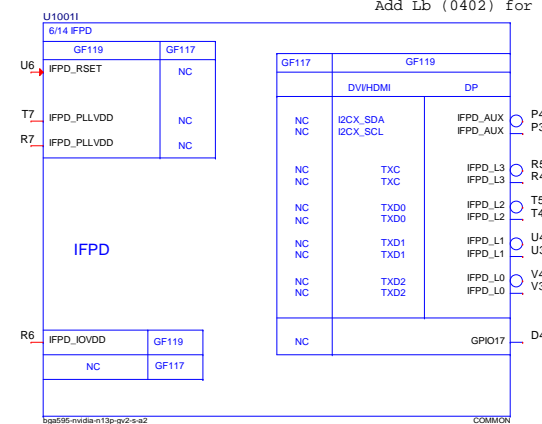




Power up sequence







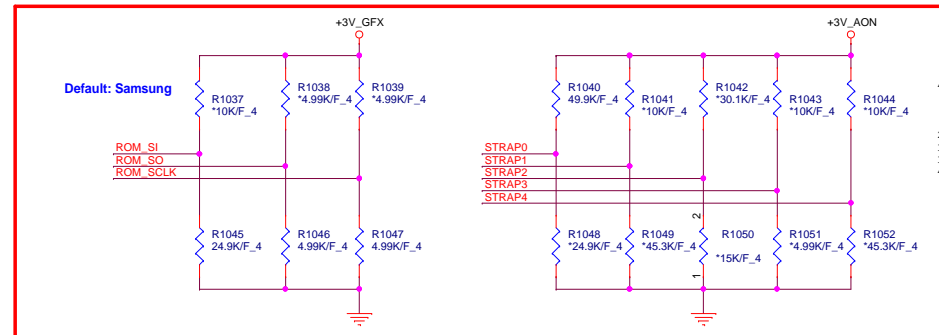
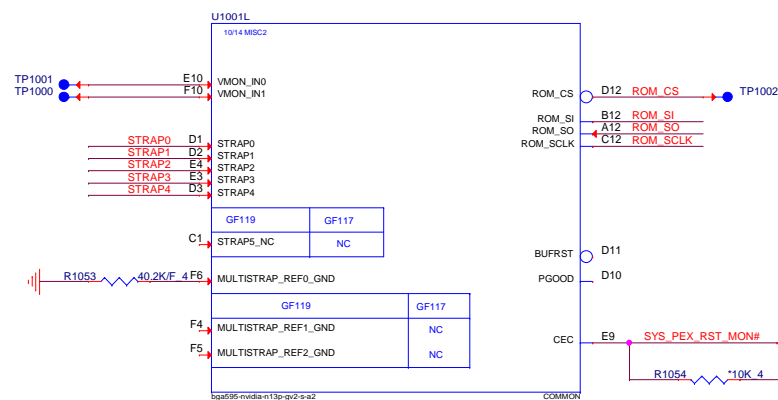
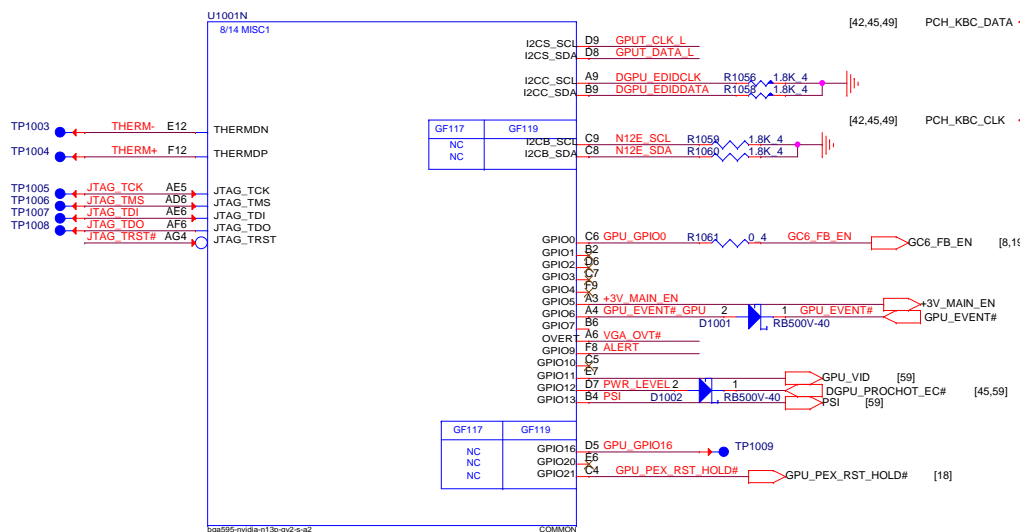


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0000	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
0011	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 - 256Mx16, 1.5V, 1Ghz/1.35V 900Mhz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY_VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



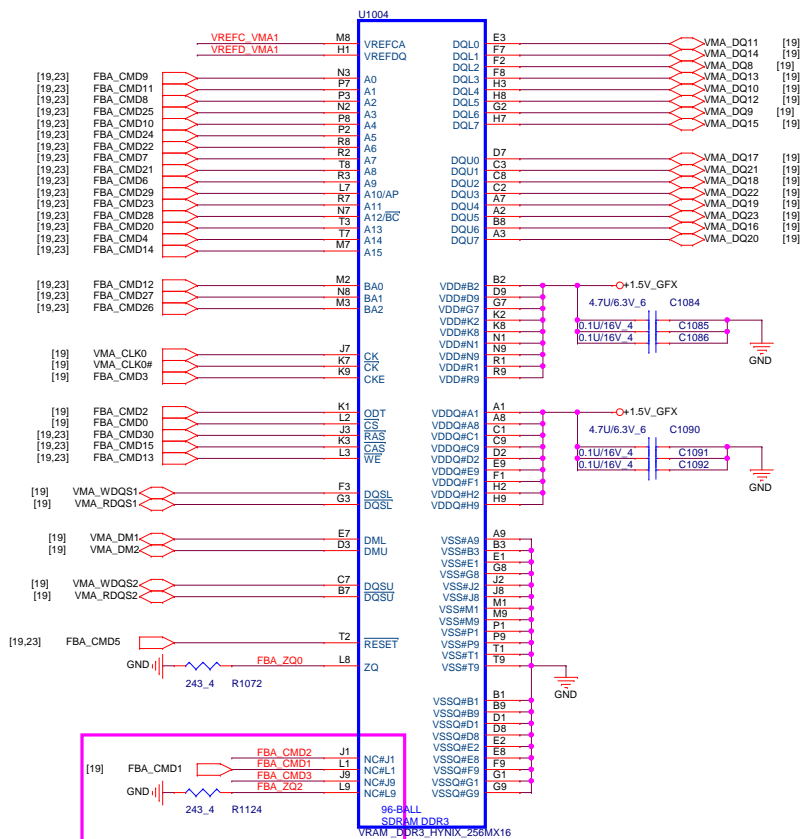
PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number	Rev
	N16S-GMR (GPIO/STRAPS)	1A
Date: Thursday, May 12, 2016	Sheet	21 of 65

Rank0

```
HYU 256Mx16, H5TC4G63AFR-11C
MIC 256Mx16, MT41J256M16HA-09
SAM 256Mx16, K4W4G1646D-BC1A
```

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



stuff R1124 for
Hynix 8Gb DDP VRAM

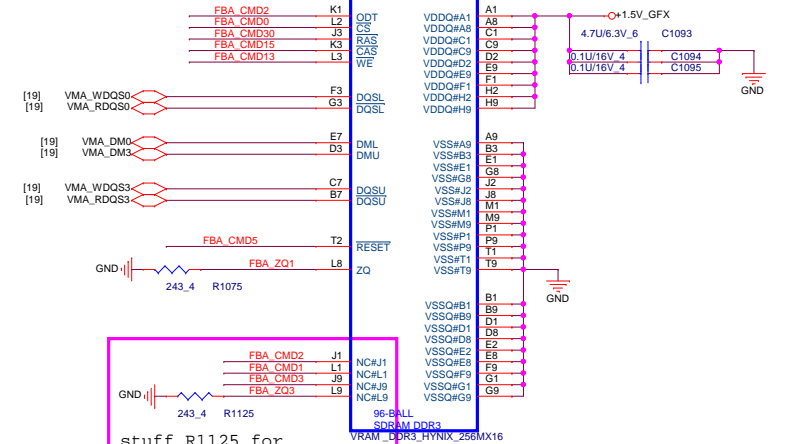
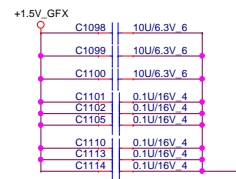
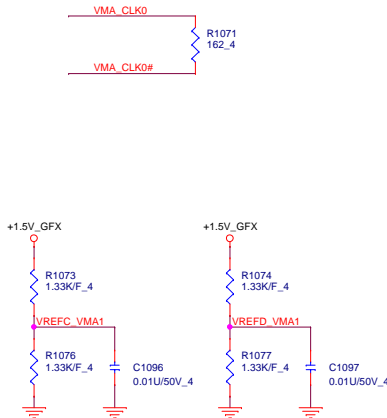
```
reserve for Hynix 8Gb DDP VRAM
```

SDDR3_BGA100

	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN FBAO ODT1	J1	NC/ODT1
SNN FBAO CKE1	J9	NC/CKE1
SNN FBAO CS1	L1	NC/CS1
SNN FBAO ZQ1	L9	NC/ZQ1

```
162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)
```



```
stuff R1125 for
Hynix 8Gb DDP VRAM
```



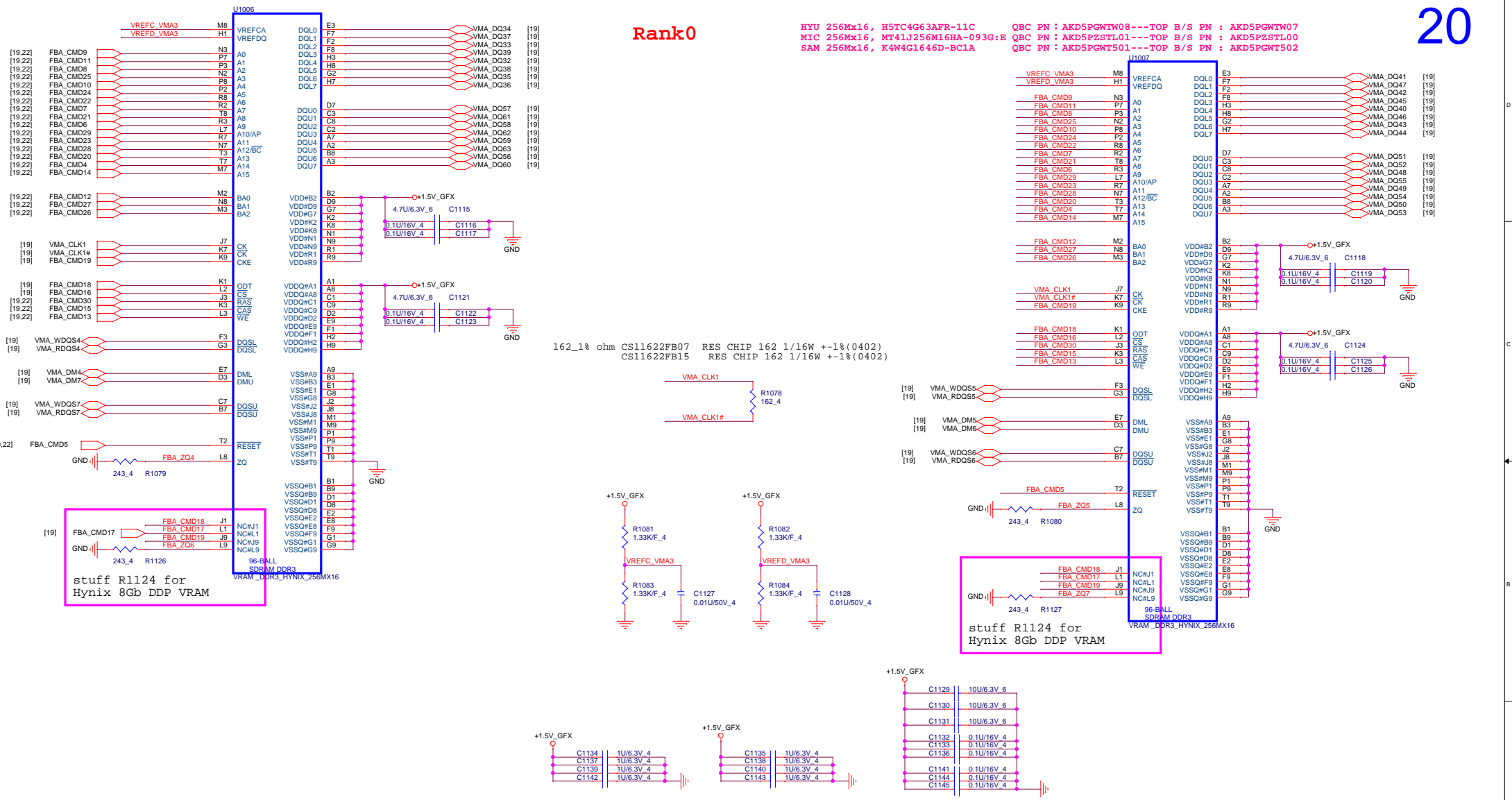
PROJECT:400 Series
Quanta Computer Inc.


Size Custom	Document Number DDR3 - RANK0	Rev 1A
Date: Thursday, May 12, 2016	Sheet	22 of 65

Rank0

HYU 256Mx16, H5TC4G63AFR-11C
MIC 256Mx16, MT41J256M16HA-093G:E
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

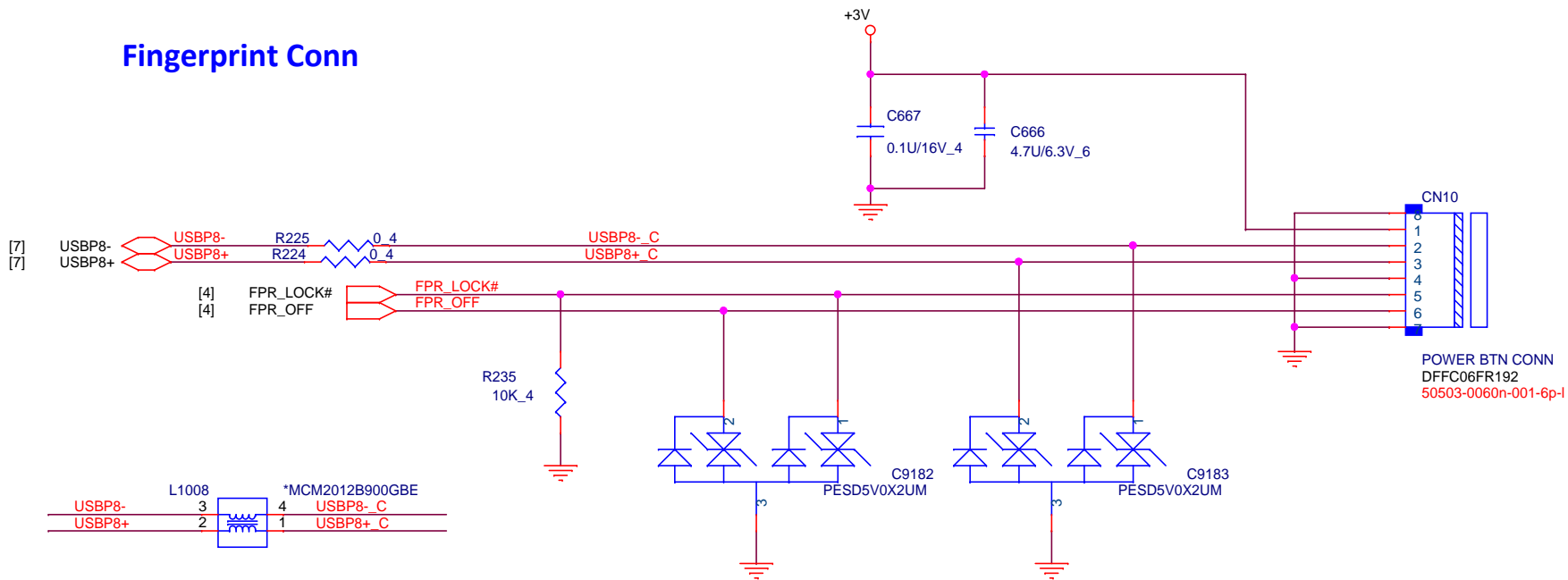





PROJECT:400 Series
Quanta Computer Inc.

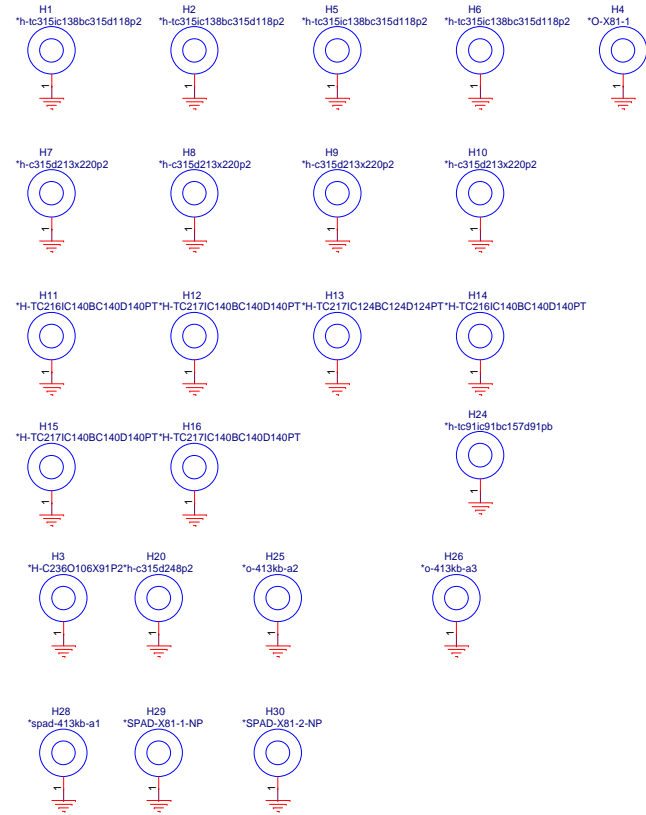
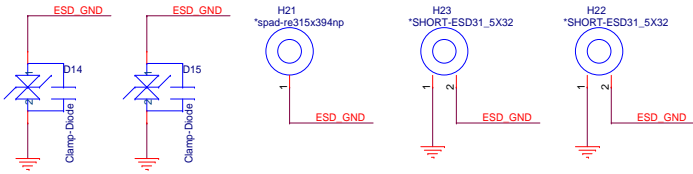
Size	Document Number	Rev
Custom	DDR3 - RANK0	1A
Date: Thursday, May 12, 2016	Sheet 23 of 85	

Fingerprint Conn

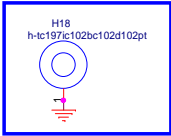


		PROJECT:400 Series Quanta Computer Inc.	
		Size Custom Document Number 24 -- FPR	Rev 1A
Date: Thursday, May 12, 2016		Sheet 24 of 65	1

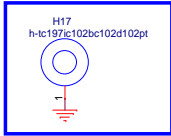
Hole



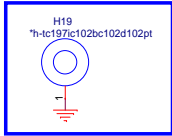
WLAN nut



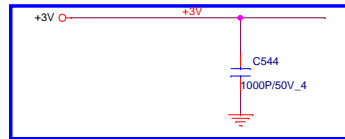
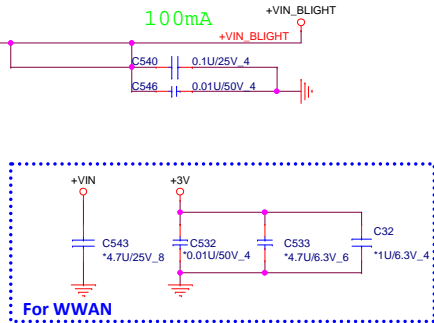
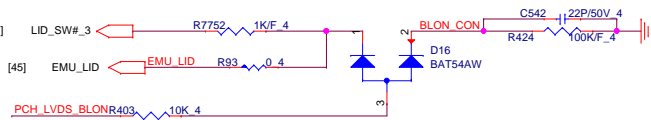
SSD nut



WWAN nut

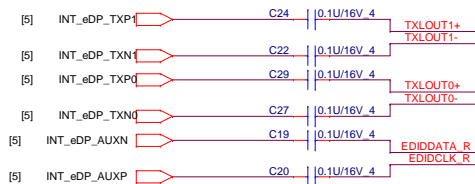
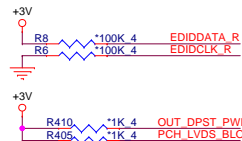
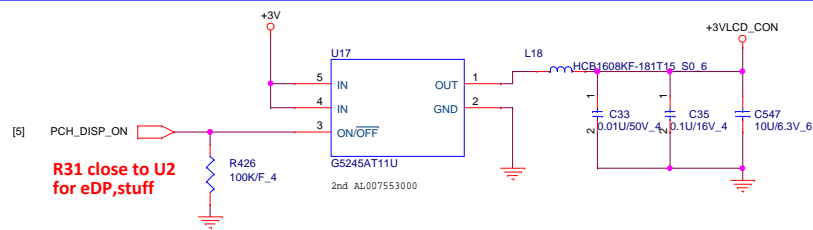


LID Switch



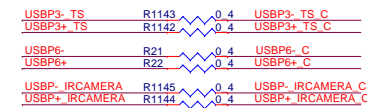
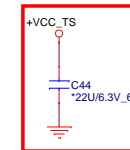
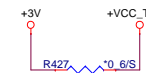
ALF@20151019:
1. Designed Reserve 4Pins for IR CCD Pin 26 to Pin29
2. Combined the +3V & +3V_CAM & +3V_IR at Pin26~25

For eDP
Close to LVDS connector

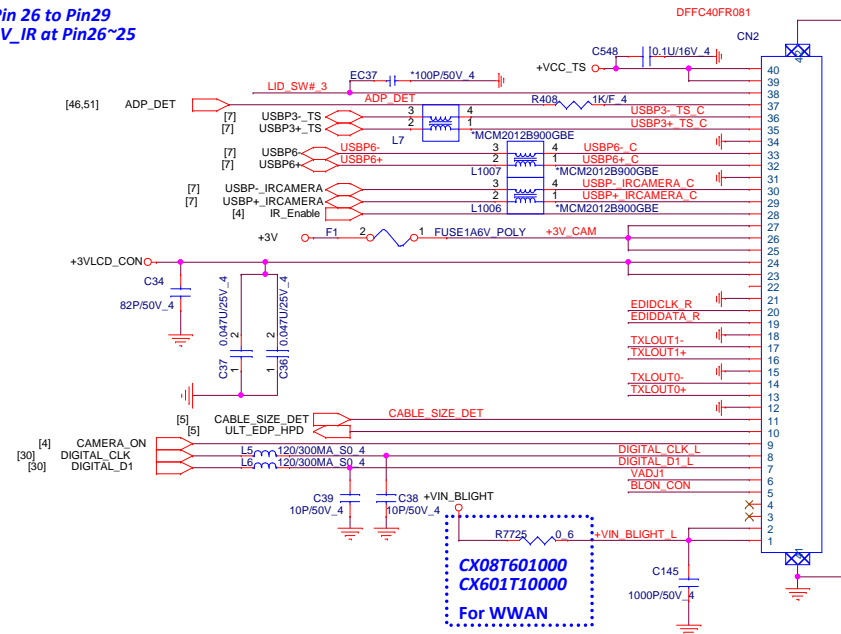


LVDS Conn.

26



GS12401-1011-9H
lvds-50671-04041-001-40p-I



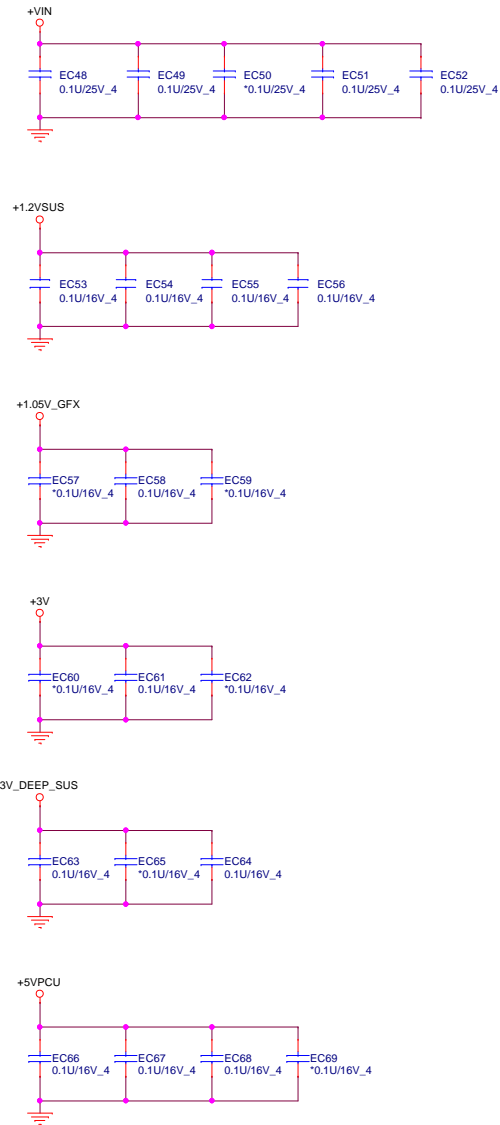
For WWAN



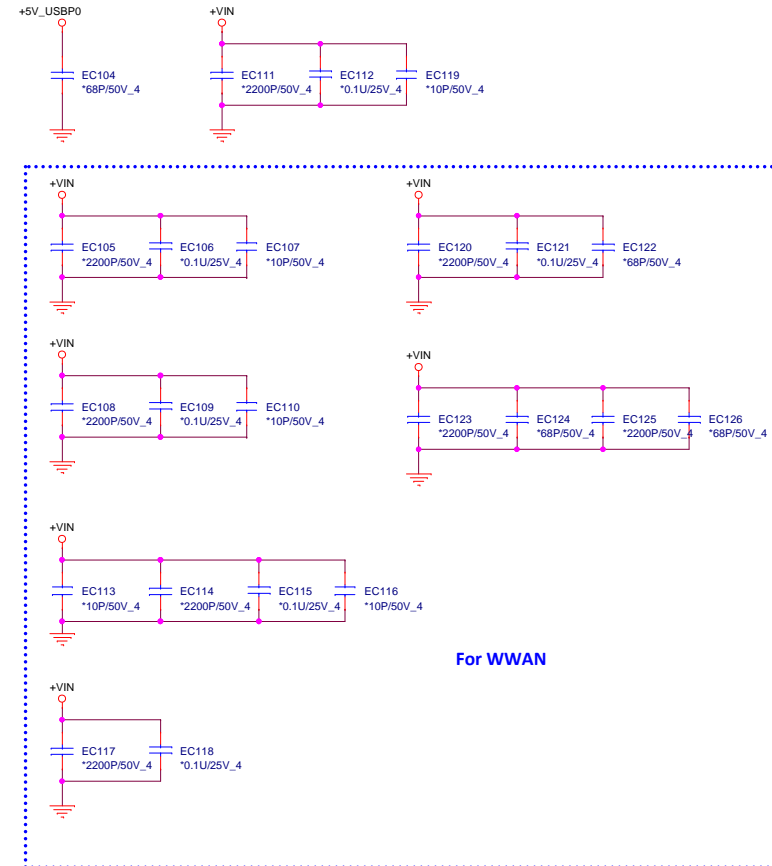
PROJECT:400 Series
Quanta Computer Inc.


Size	Document Number	Rev
Custom	26 - LCD CONN/LID/CAM/D-MIC	1A
Date: Thursday, May 12, 2016	Sheet 26 of 65	

EMI CAP



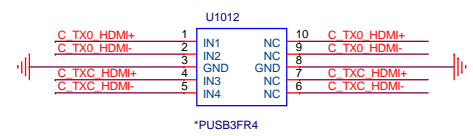
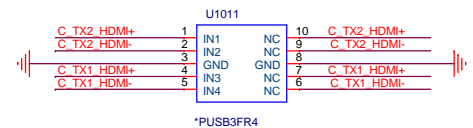
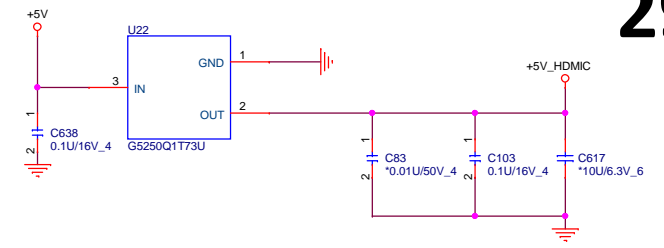
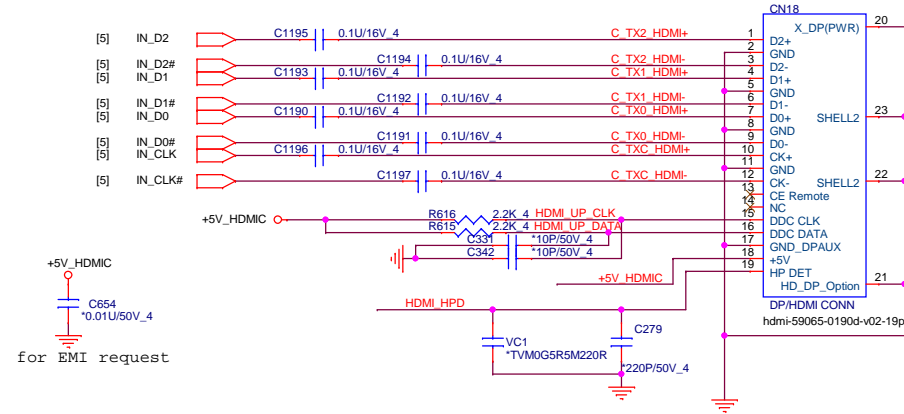
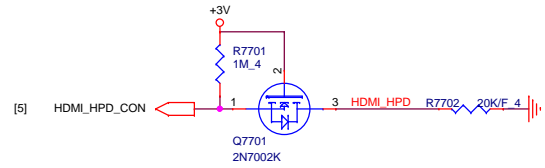
RF Cap



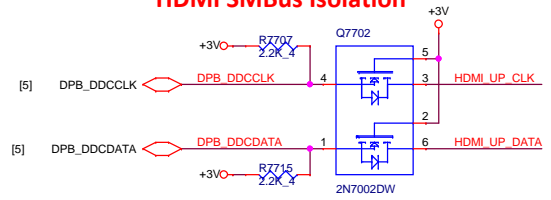
 NB5	PROJECT:400 Series		
	Quanta Computer Inc.		
	Size Custom	Document Number 28 – REPEATER PS8407A	Rev 1A
	Date: Thursday, May 12, 2016	Sheet 28 of 65	

EMI Solution

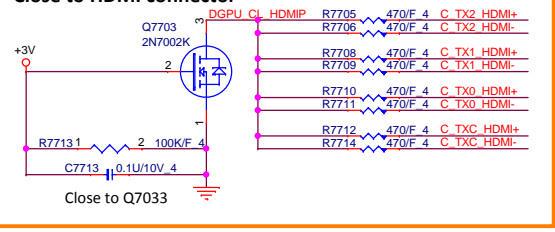
C_TX2_HDMI+	R208	120/F 4	C_TX2_HDMI-
C_TX1_HDMI+	R194	120/F 4	C_TX1_HDMI-
C_TX0_HDMI+	R178	120/F 4	C_TX0_HDMI-
C_TXC_HDMI+	R221	120/F 4	C_TXC_HDMI-



HDMI SMBus Isolation



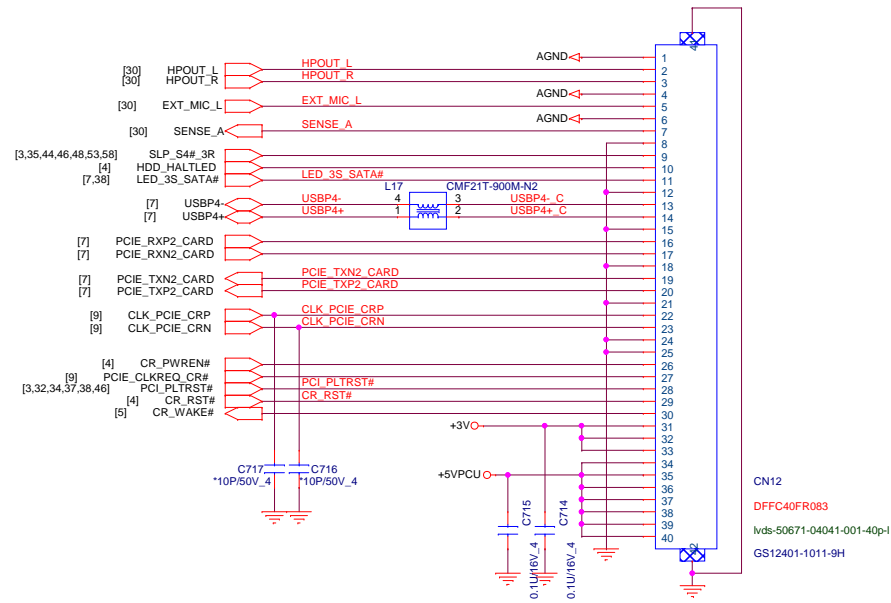
Close to HDMI connector




PROJECT:400 Series
Quanta Computer Inc.

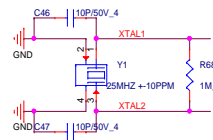
Size Custom	Document Number	Rev 1A
	29 -- HDMI CONNECTOR	
Date: Thursday, May 12, 2016	Sheet 29 of 65	

USB/Card Reader/Headphone_Mic Combo Jack Daugther Board Connector



			PROJECT:400 Series Quanta Computer Inc.	
Size	Custom	Document Number	31 -- DAUGHTER BOARD CONN.	Rev
				1A
Date: Thursday, May 12, 2016		Sheet 31 of 65		

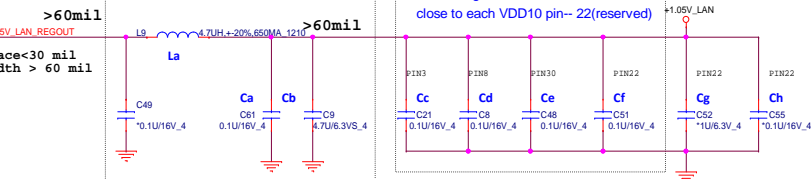
LAN & RJ45



Power trace Layout 寬度> 60mil

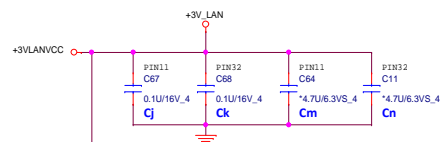
* Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 22, 8 , 30

- * Place Cg,Ch close to each VDD10 pin-- 22(reserved)



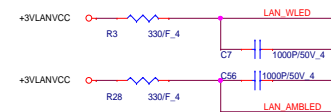
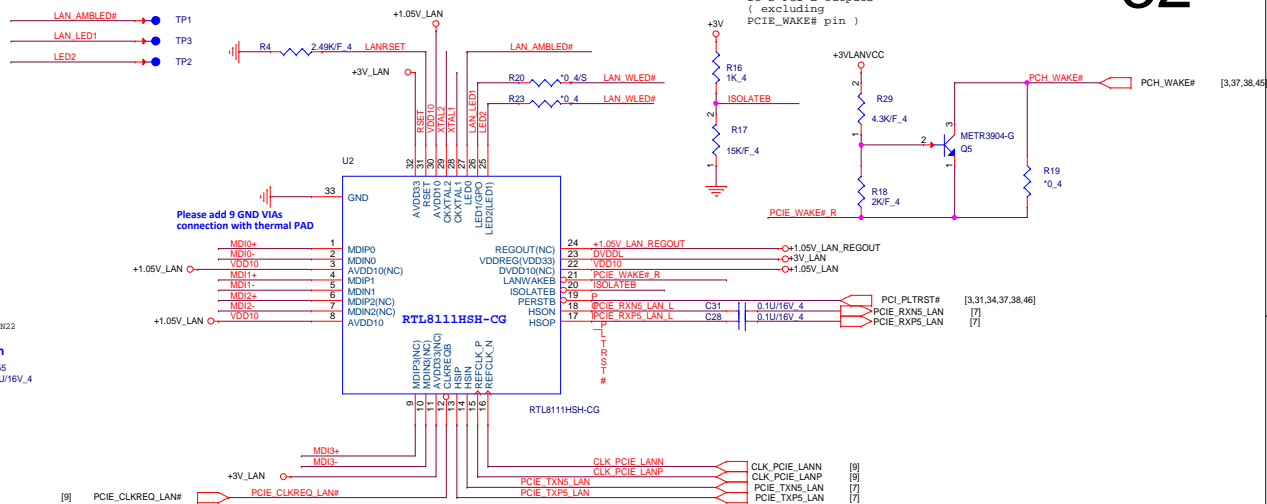
For SWR mode
 Stuff La, Ca ,Cb
 NA : Ra, Ci

- * Place Cj and Ck, close to each VDD33 pin-- 11, 32
- * For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

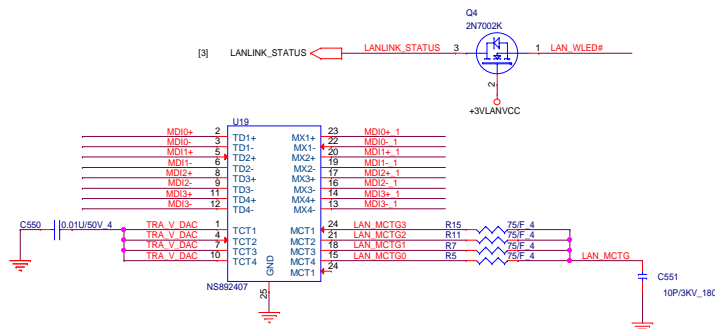
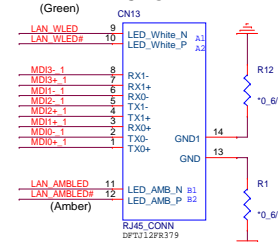


For SWR mode
Stuff Co, Cp

Remove For Not Using SWR mode



RJ45

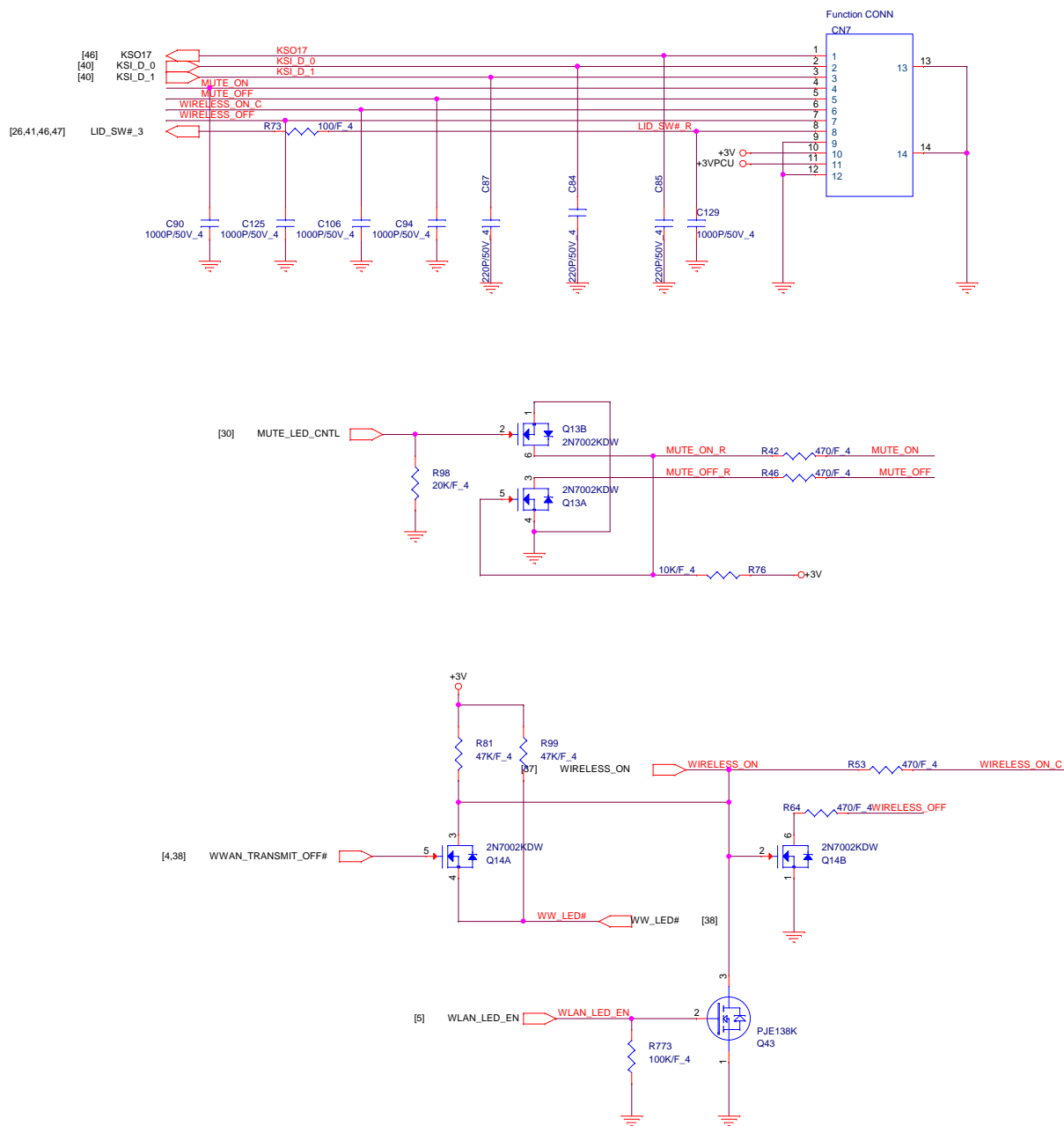



For GiGA BOT:GST5009B LE DB0Z06LAN00

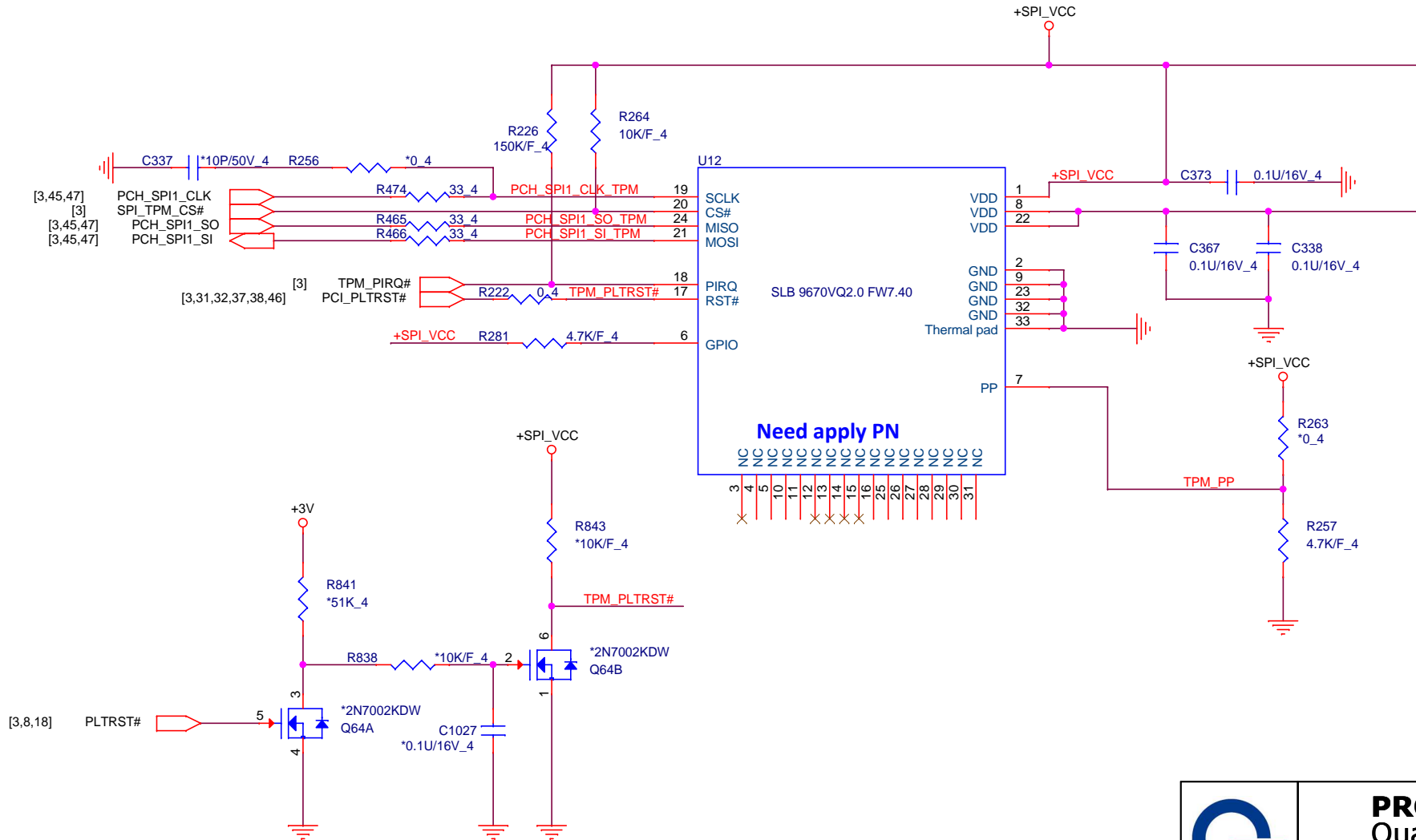
FCE :NS892407 ,DB0LL1LAN00


[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,33,34,36,38,42,44,45,47,51,56,58,59,63]

[58] +3V
+3VLAVCC



			PROJECT:400 Series Quanta Computer Inc.		
Size Custom	Document Number 33 – Function Conn.		Rev 1A		
Date: Thursday, May 12, 2016		Sheet	33	of	65

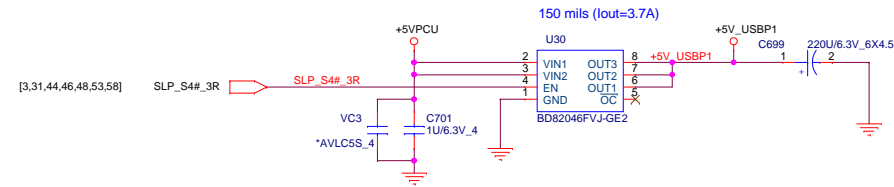
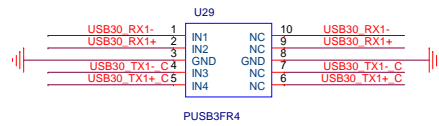
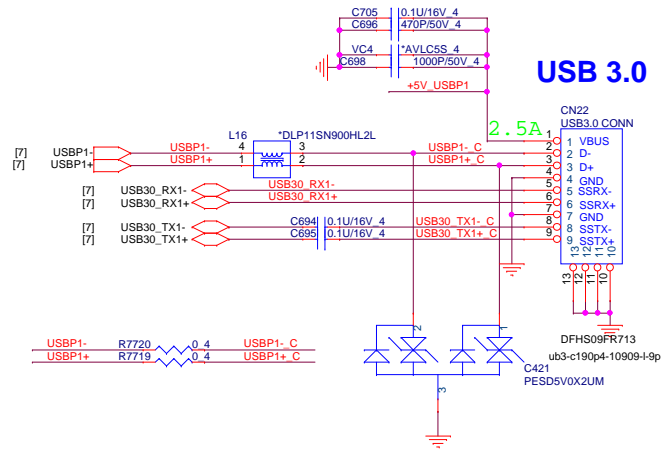




PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 34 -- TPM SLB9670_QFN	Rev 1A
Date: Thursday, May 12, 2016		Sheet 34 of 65

USB 2.0/3.0 Combo



[28,31,44,49,50,51,52,53,54,56,57,58,59,60,61,63]

+5VPCU

[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63]

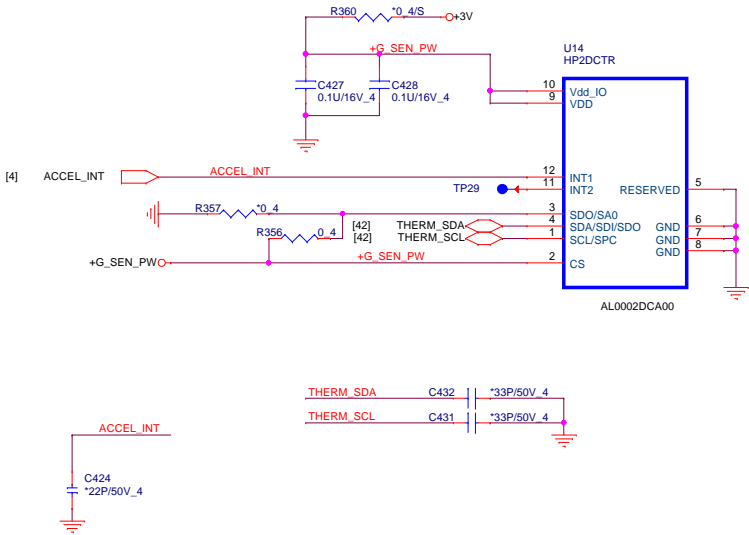
+3VPCU



PROJECT:400 Series
Quanta Computer Inc.


Size Custom	Document Number 35 – USB3.0 x2	Rev 1A
Date: Tuesday, May 17, 2016		Sheet 35 of 65

Accelerometer Sensor



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,38,42,44,45,47,51,56,58,59,63] +3V

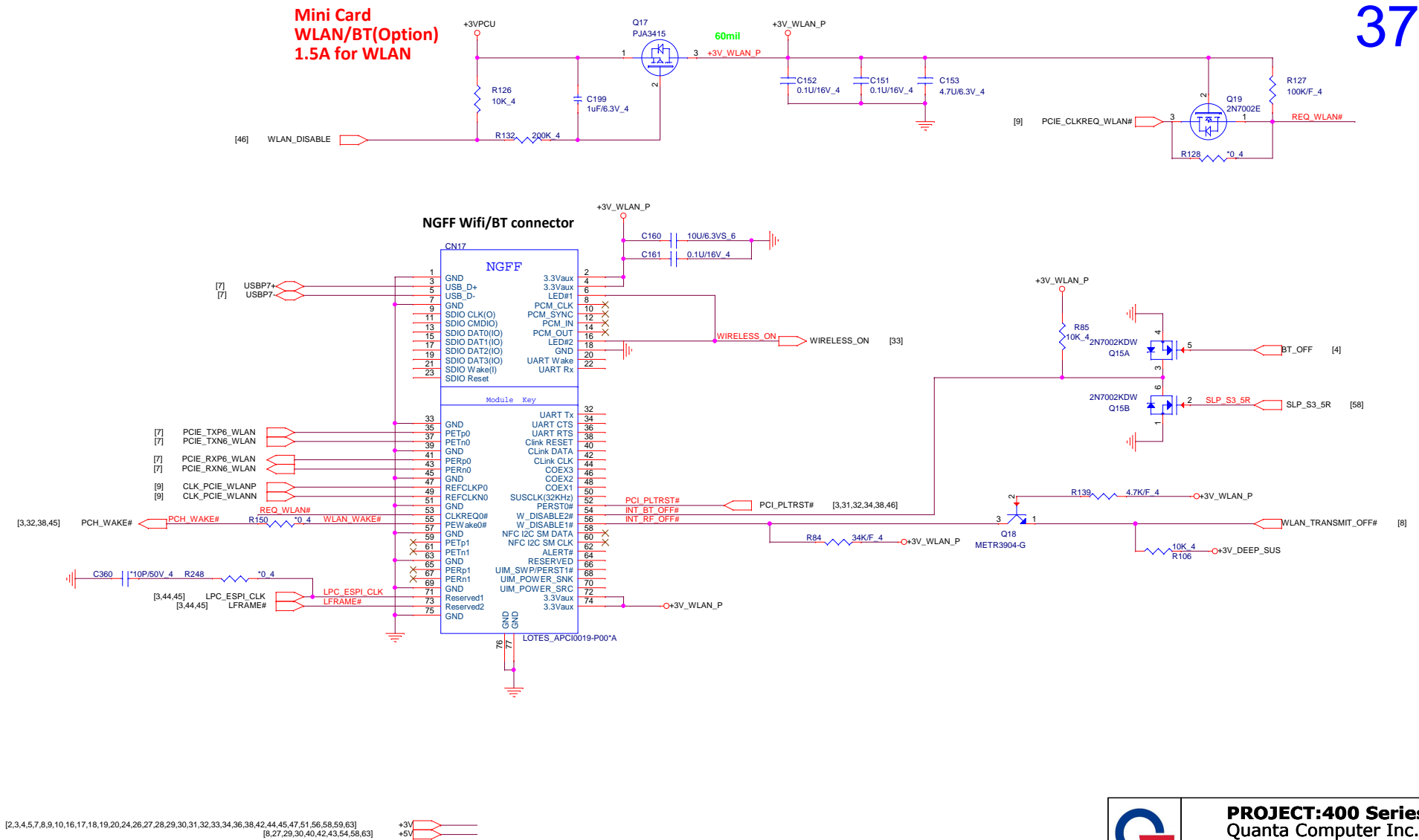
[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63] +3VPCU

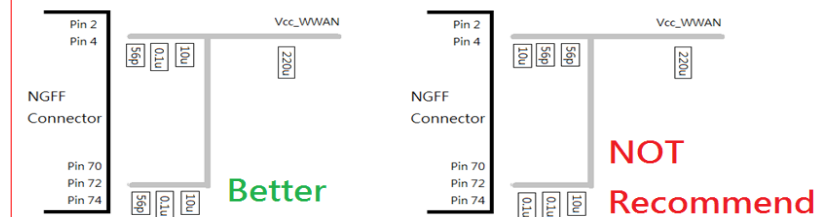
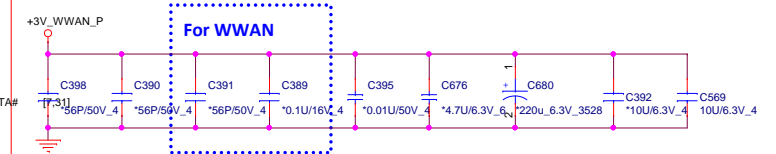
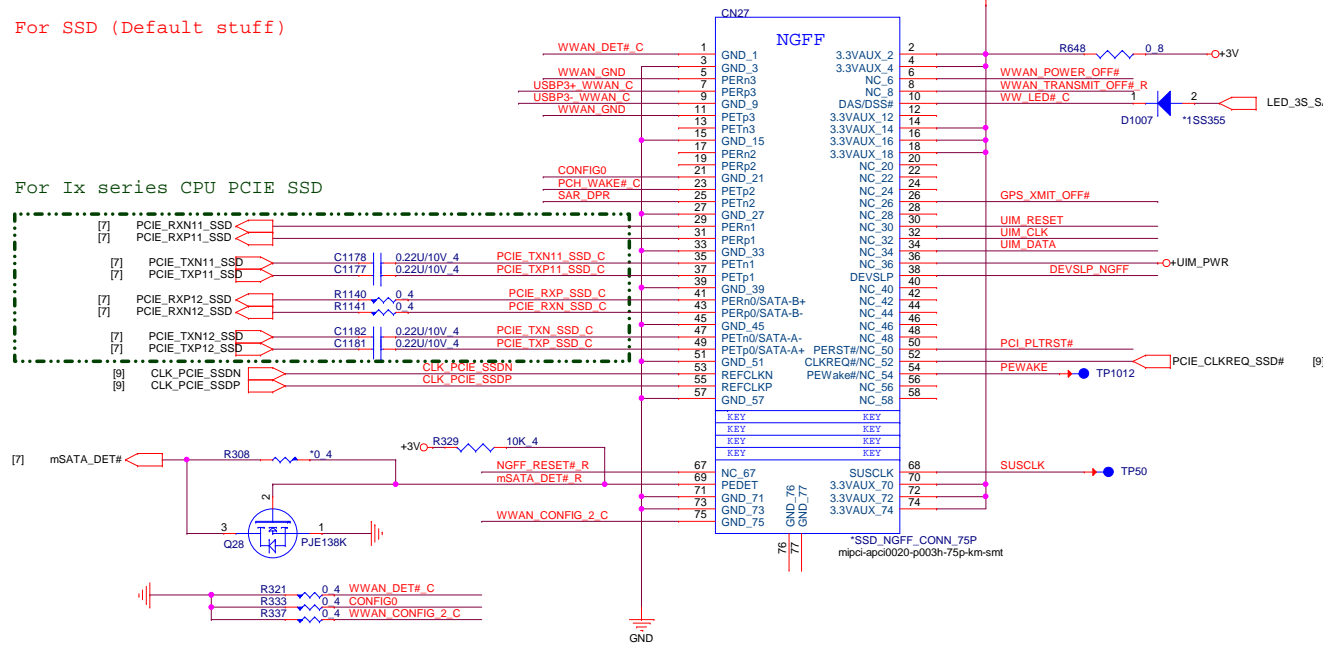
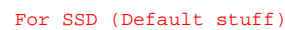
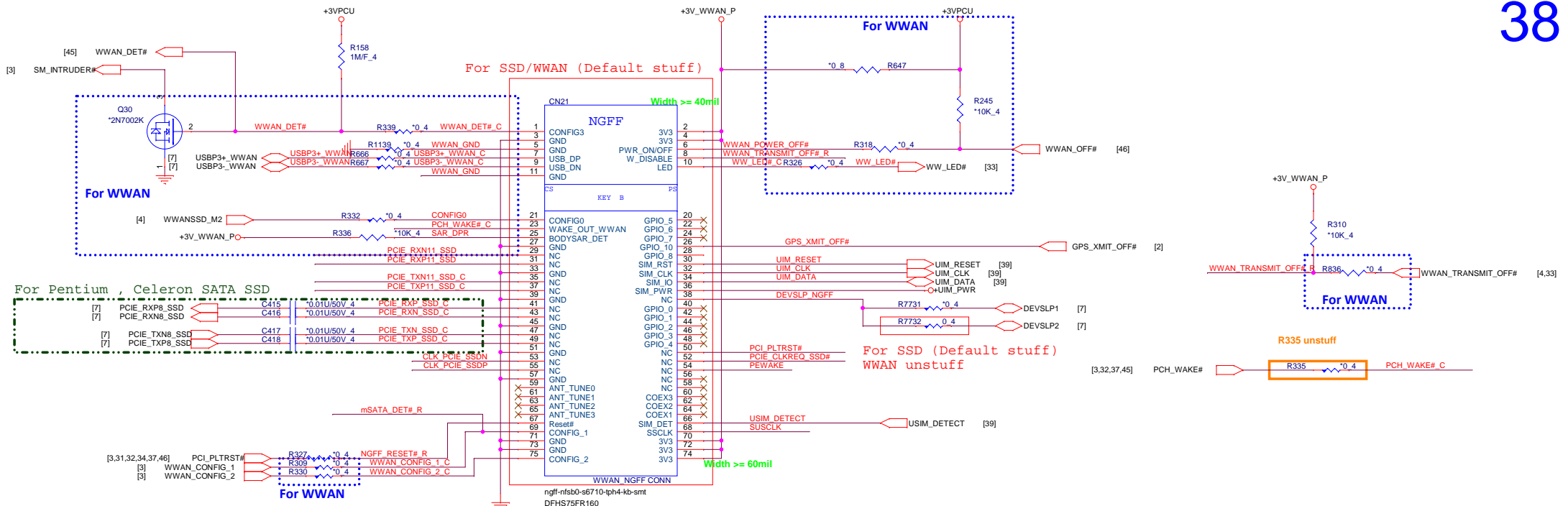


NB5

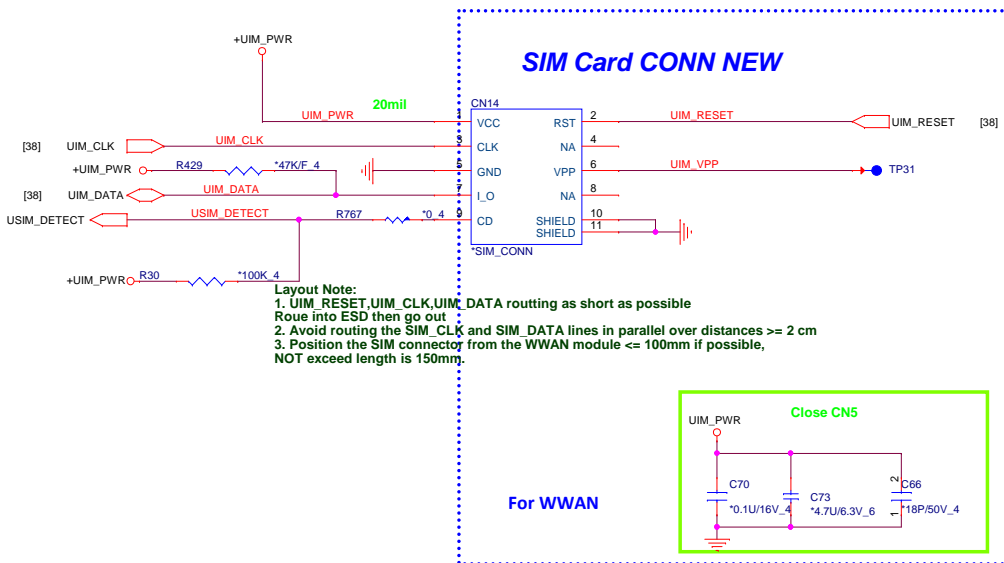
PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 36 -- TS and Accelerometer	Rev 1A
Date: Thursday, May 12, 2016		Sheet 36 of 65





+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low

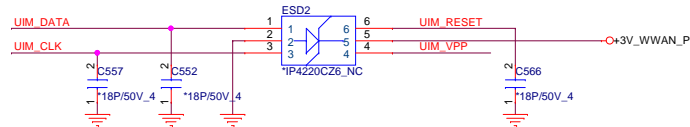


Trace Length and Routing^u

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.^u
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.^u
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.^u
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.^u

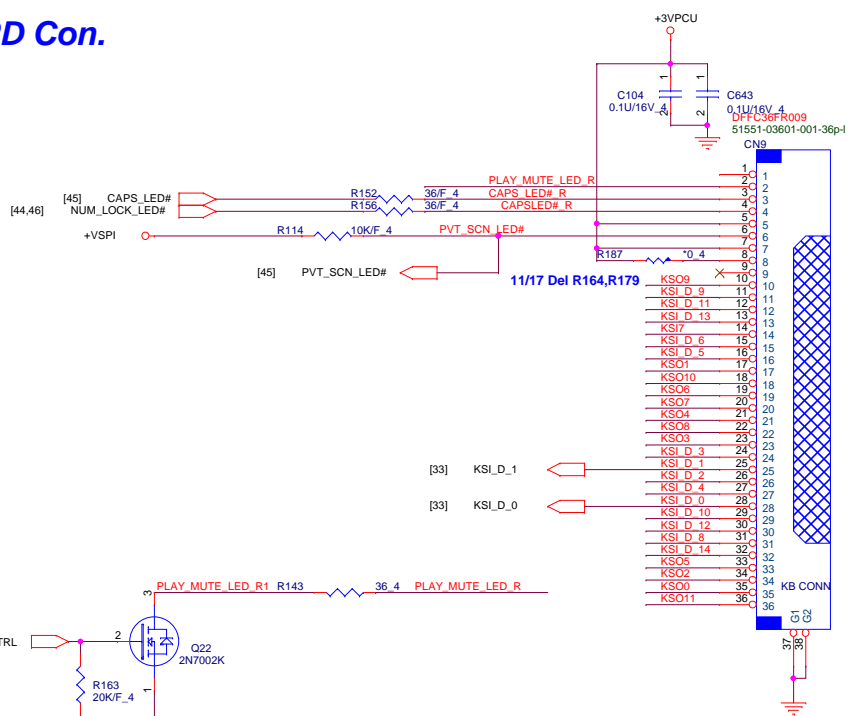
SIM Power^u

- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.^u
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.^u

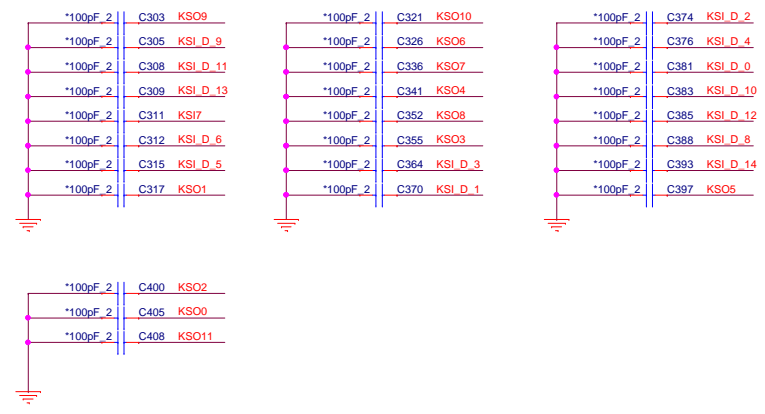
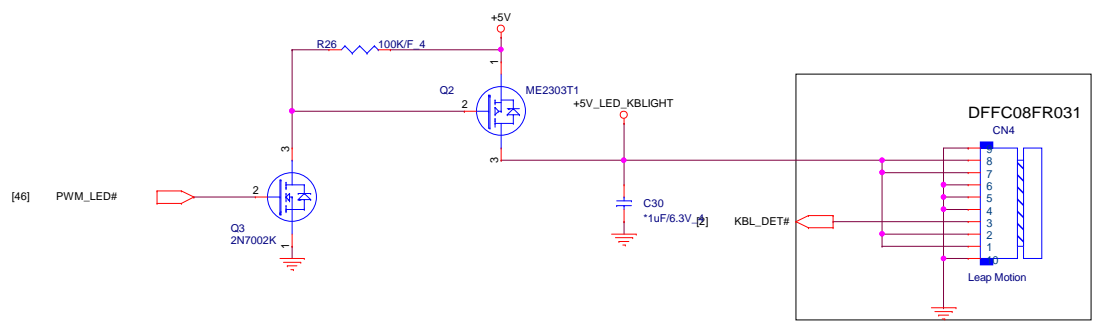
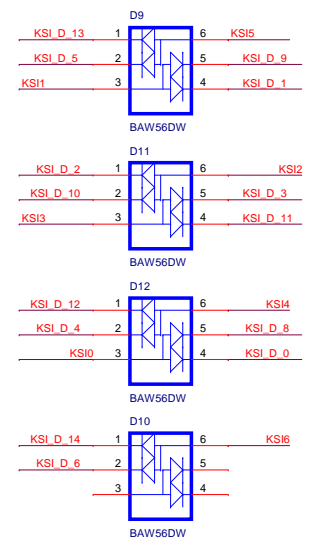
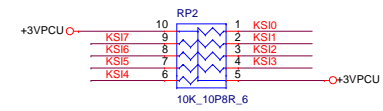


PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 39 -- SIM CARD/ RF cap	Rev 1A
Date: Thursday, May 12, 2016	Sheet 39 of 65	




KEYBOARD PULL-UP



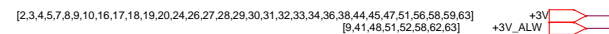
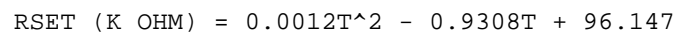
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]
[8,27,29,30,42,43,54,58,63]



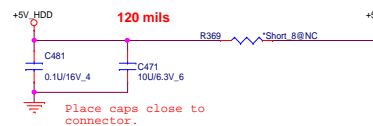
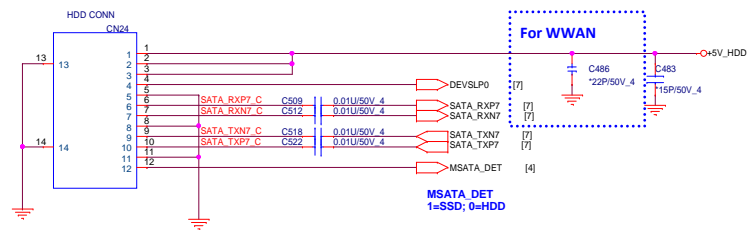


PROJECT:400 Series
Quanta Computer Inc.

Size Custom	Document Number 40 - KB/ KB light CONN	Rev 1A
Date: Thursday, May 12, 2016		Sheet 40 of 65



SATA-HDD



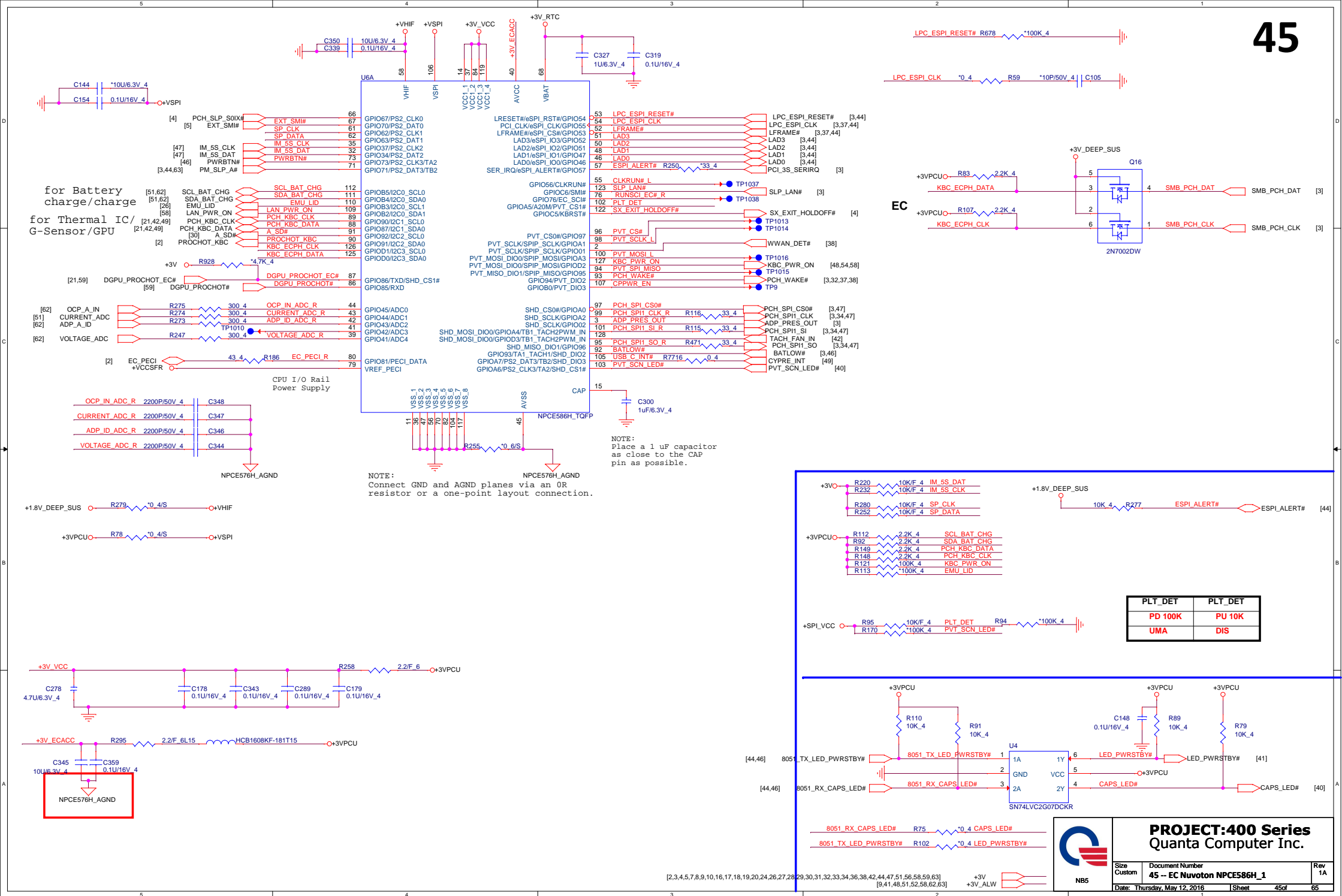
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]
[8,27,29,30,40,42,54,58,63]

+3V
+5V

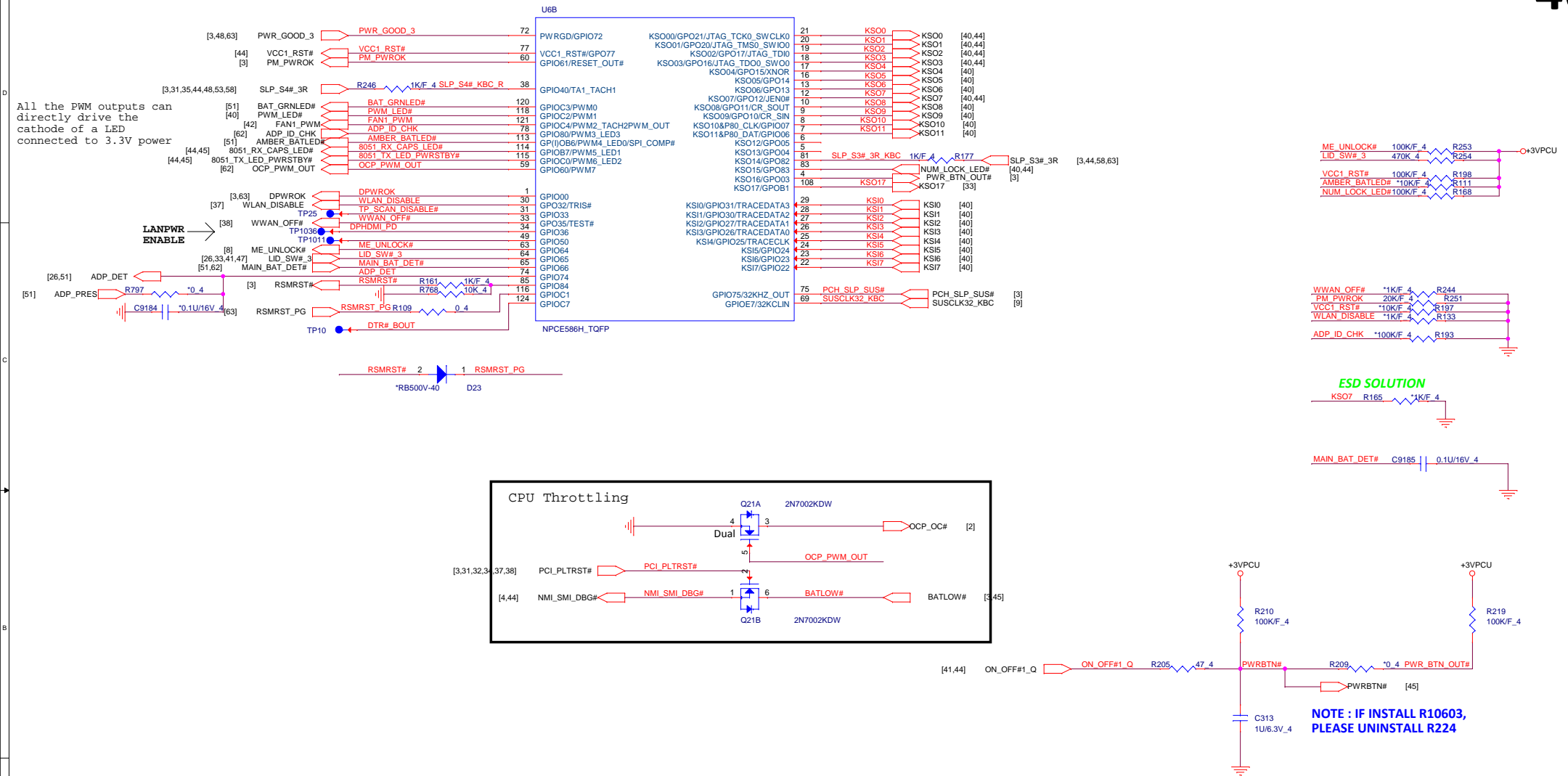
I'm from VIETNAM sualaptop365



LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R658	Ra INSTAL	UNINSTAL
R646	Rb INSTAL	UNINSTAL
R659	Rc INSTAL	UNINSTAL
R656	Rd INSTAL	UNINSTAL
R649	Re INSTAL	UNINSTAL
R657	Rf INSTAL	UNINSTAL
R249	Rg INSTAL	UNINSTAL
R147	Rh INSTAL	UNINSTAL
R120	Ri INSTAL	UNINSTAL
R276	Rj INSTAL	UNINSTAL
R678	Rk UNINSTAL	INSTAL

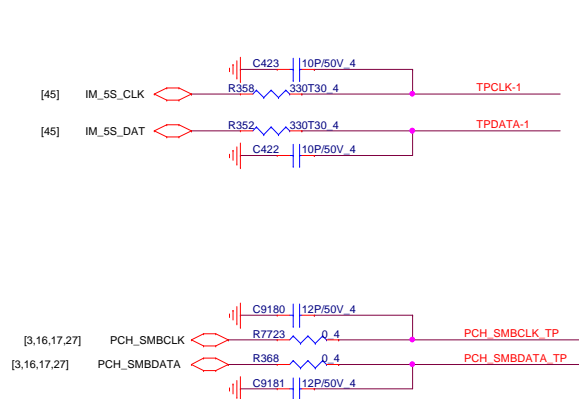
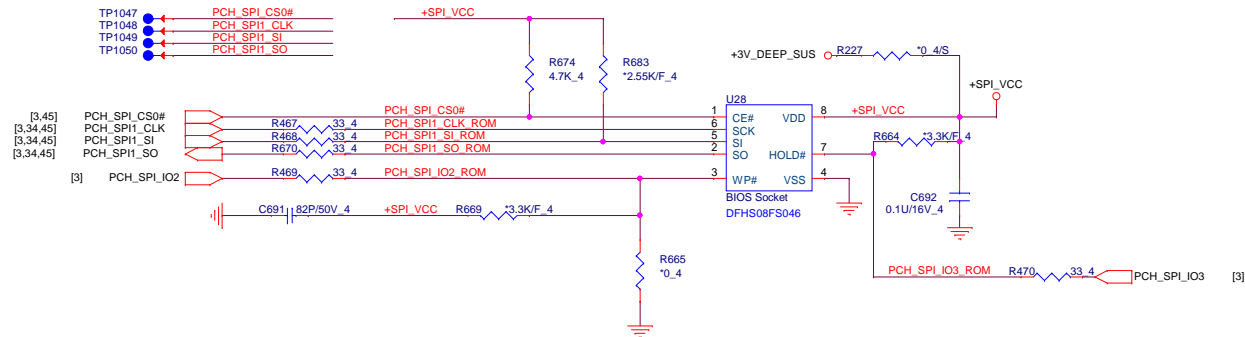


All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power



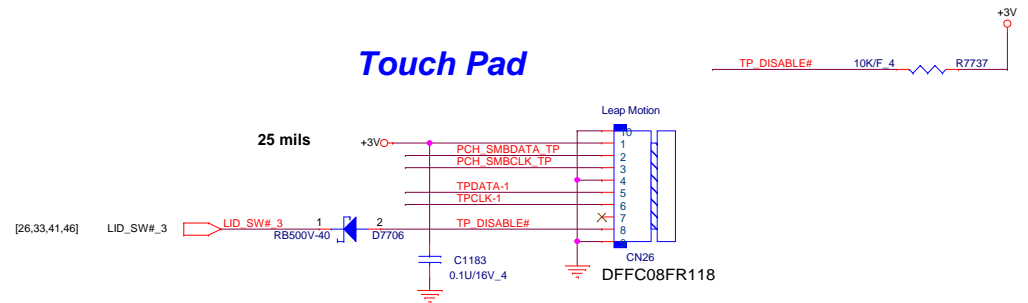
Vender	Size	P/N
GD	128MB	AKE2DF0KQ00
Winbond	128MB	AKE3DZKNK00
Socket		DFHS08FS046


PCH SPI ROM(CLG)

PCH 6*5mm WSON 16M
SPI ROM Socket

CLICK PAD
Address: 0x20(7 bit)

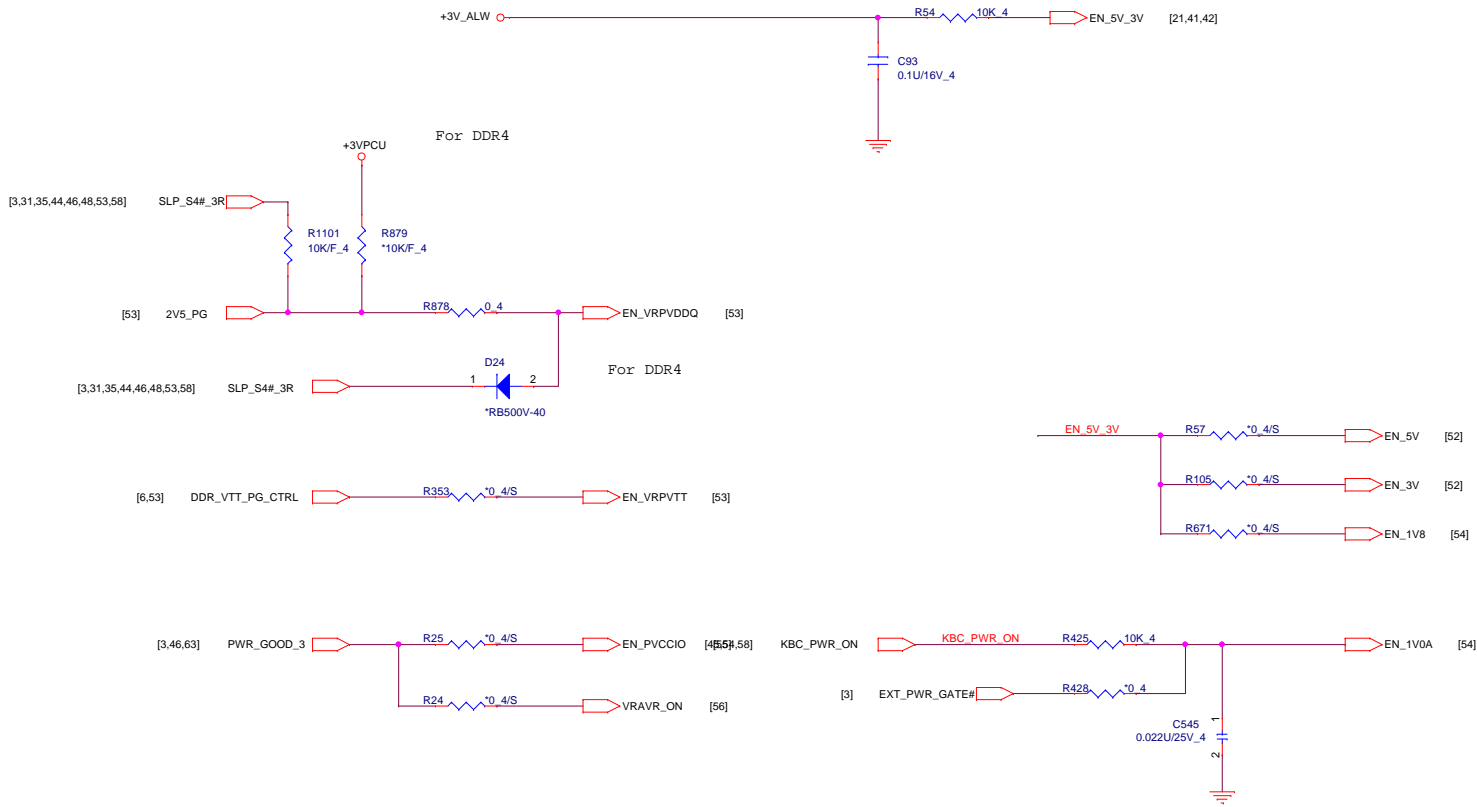
Touch Pad




 NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 47 - Flash(KBC+PCH)	Rev 1A
	Date: Thursday, May 12, 2016	Sheet 47 of 65	

400 series 1001

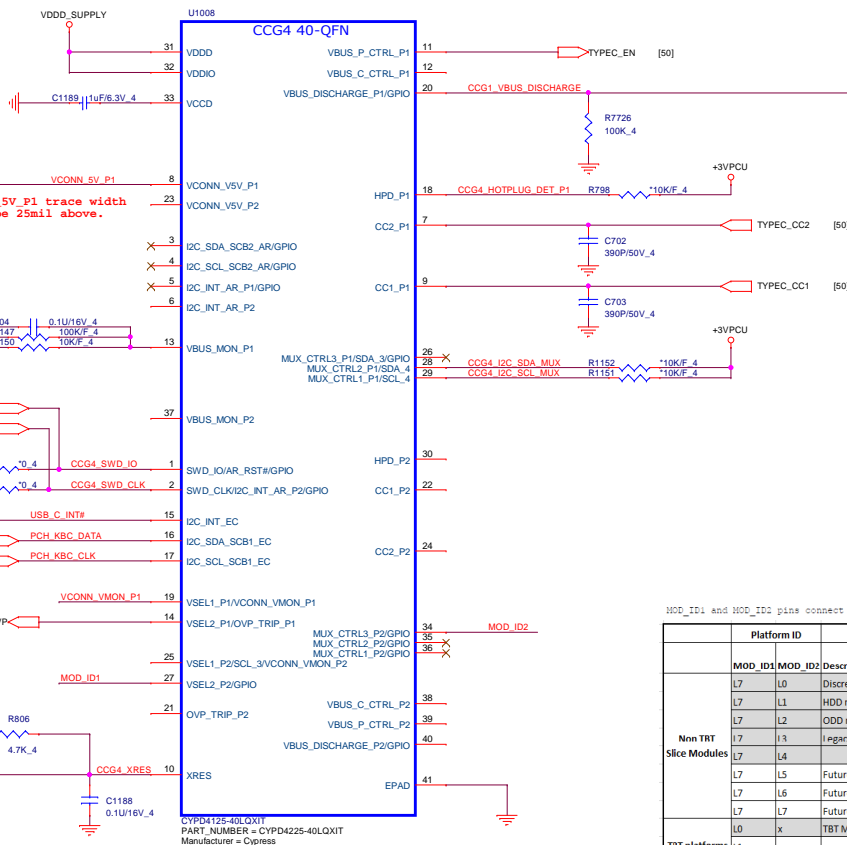
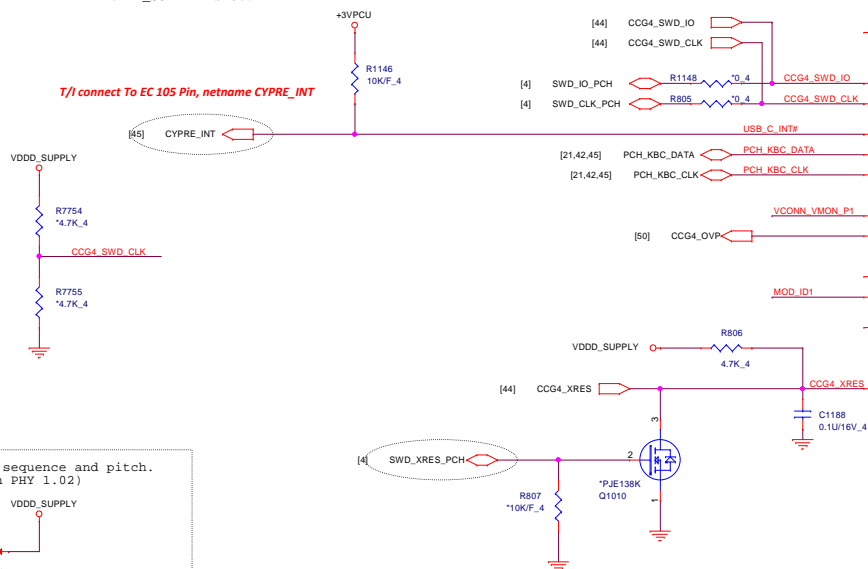
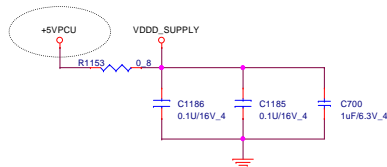
POWER TO EE NET NAME CONNECTION



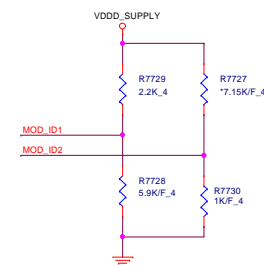


NB5

PROJECT:400 Series Quanta Computer Inc.		
Size Custom	Document Number 48 -- POWER ENABLE	Rev 1A
Date: Thursday, May 12, 2016	Sheet	48 of 65



MOD_ID	Pull high	Pull down
L0	None	1K
L1	7.1K	1K
L5	3.09K	5.1K
L6	2.2K	5.9K



MOD ID1 and MOD ID2 pins connect to ADC in CCG4

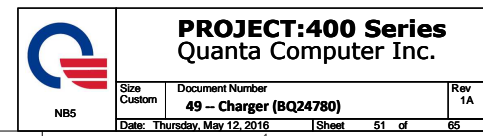
	Platform ID		Dual Port	Single Port			
	MOD_ID1	MOD_ID2	Description (Dual port)	Dual Port CFGID	Description (Single)		Single Port CFGID
Non TBT Slice Modules	L7	L0	Discrete GFX module for Slice	CFG0			L0 = 0V
	L7	L1	HDD module for Slice	CFG1			L1 = VDD0/3
	L7	L2	ODD module for Slice	CFG1			L2 = 2* VDD0/3
	L7	L3	Legacy I/O module for Slice	CFG1			L3 = 3* VDD0/3
	L7	L4			Communication	CFG0	L4 = 4* VDD0/3
	L7	L5	Future use				L5 = 5* VDD0/3
	L7	L6	Future use				L6 = 6* VDD0/3
	L7	L7	Future use				L7 = 7* VDD0/3
TBT platforms	L0	x	TBT Module for Slice	CFG2			
	L1	x			Slice Gen2	CFG1	
	L2	x			800 & 600, AIO Addon Card	CFG2	
Non TBT Desktop Platforms	L5	L0	Slice Gen1 & Gen2	CFG3	Slice Gen1	CFG3	
	L5	L1	800 & 600 Series	CFG4	800 & 600, 400 Series (DFP)	CFG4	
	L5	L2	Future		800 & 600 (DFP+DP)	CFG5	
Non TBT Notebook Platforms	L6	L0	DRP iDP on two ports	CFG5	DFP only	CFG4	
	L6	L1			DFP + DP on single port	CFG5	



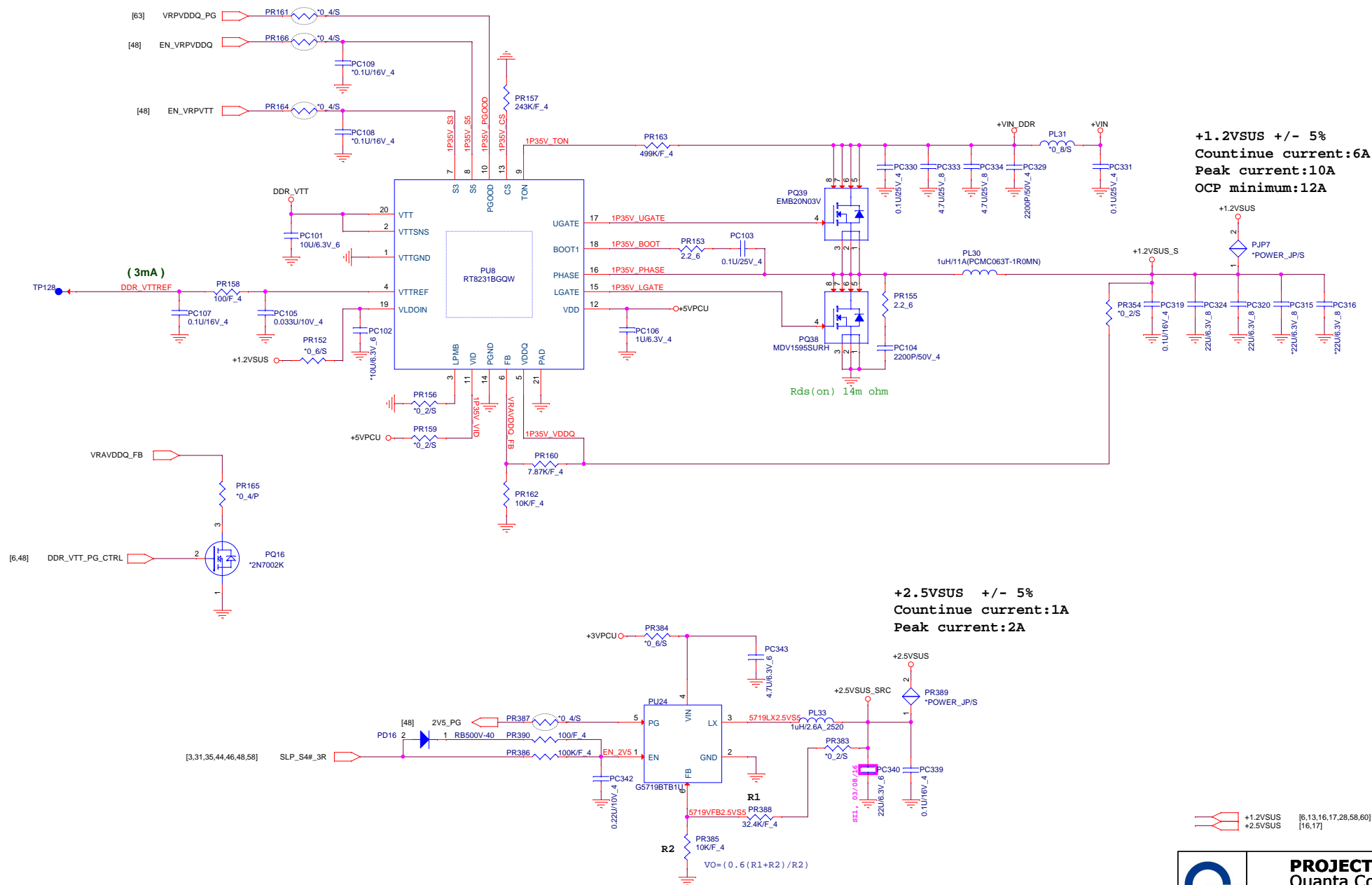
PROJECT:400 Series
Quanta Computer Inc.

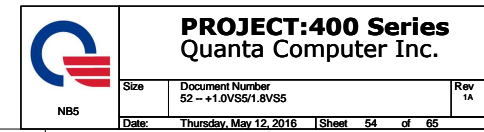
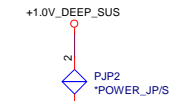
Size	Document Number	R
	49 -- Cypress CCG1	
Date:	Friday, May 20, 2016	Sheet 49 of 65





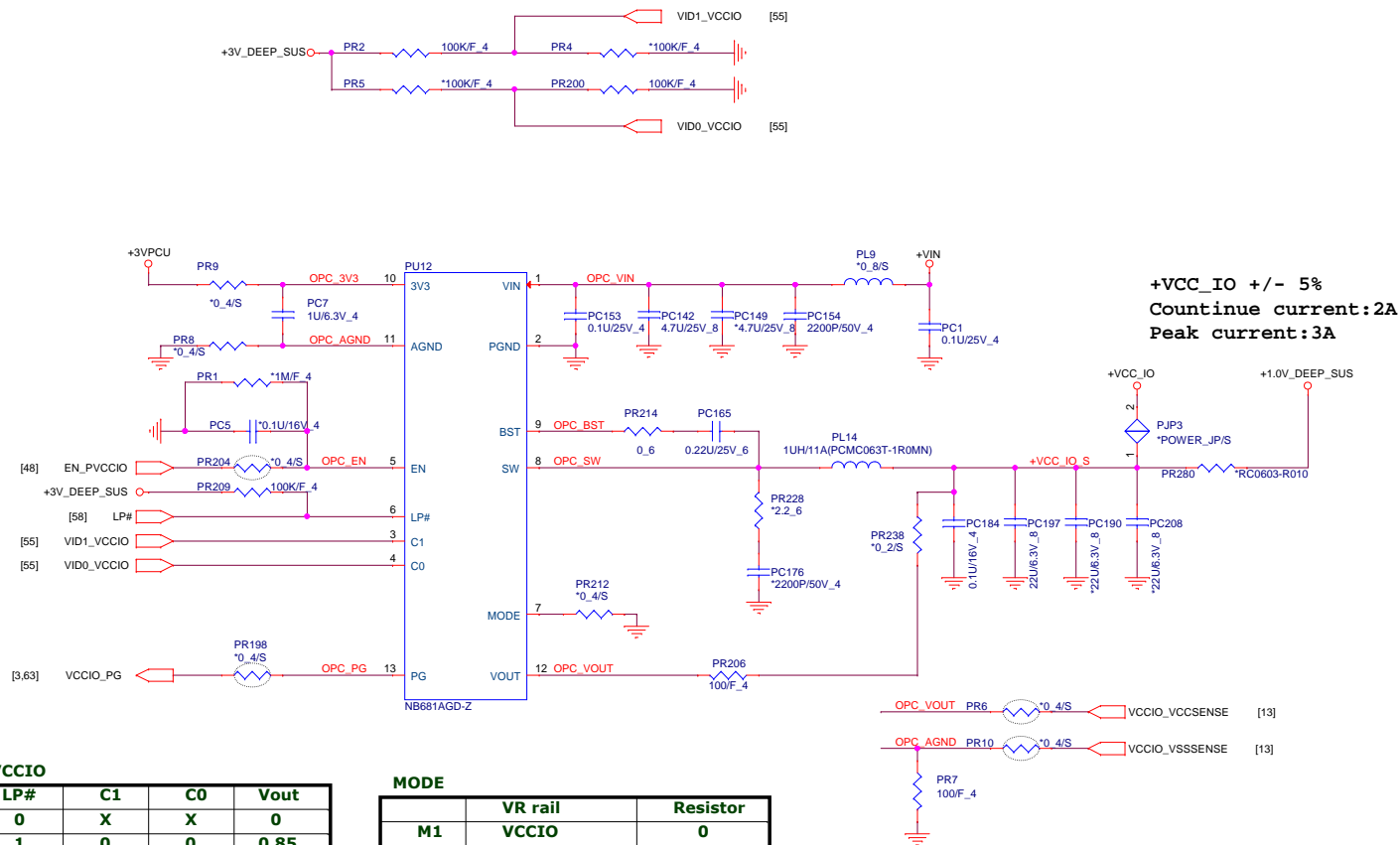
I'm from VIETNAM **sualaptop365**



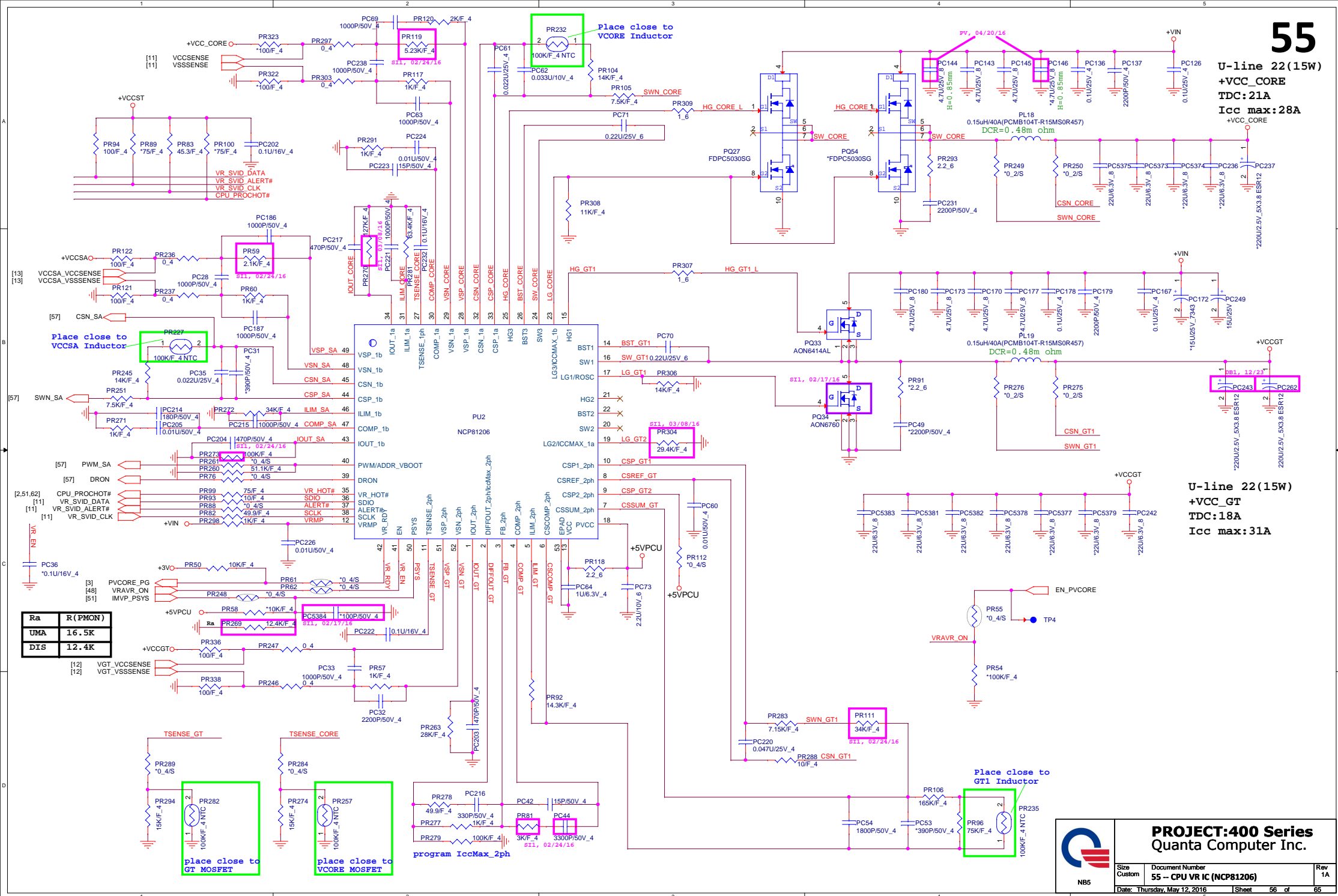


[26,28,44,51,52,53,54,56,57,58,59,61,66]
[9,41,48,51,52,58,62,63]
[5,13]

+VIN
+3V_ALW
+VCC_IO

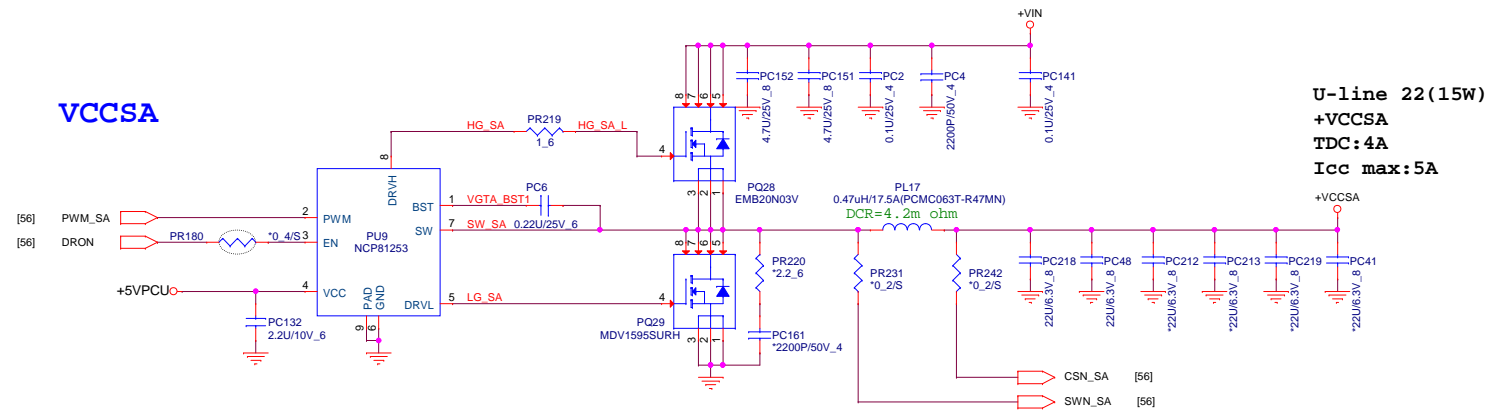


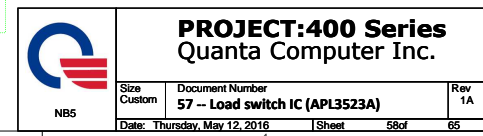
U-line 22(15W)
+VCC_CORE
TDC:21A
Icc max:28A

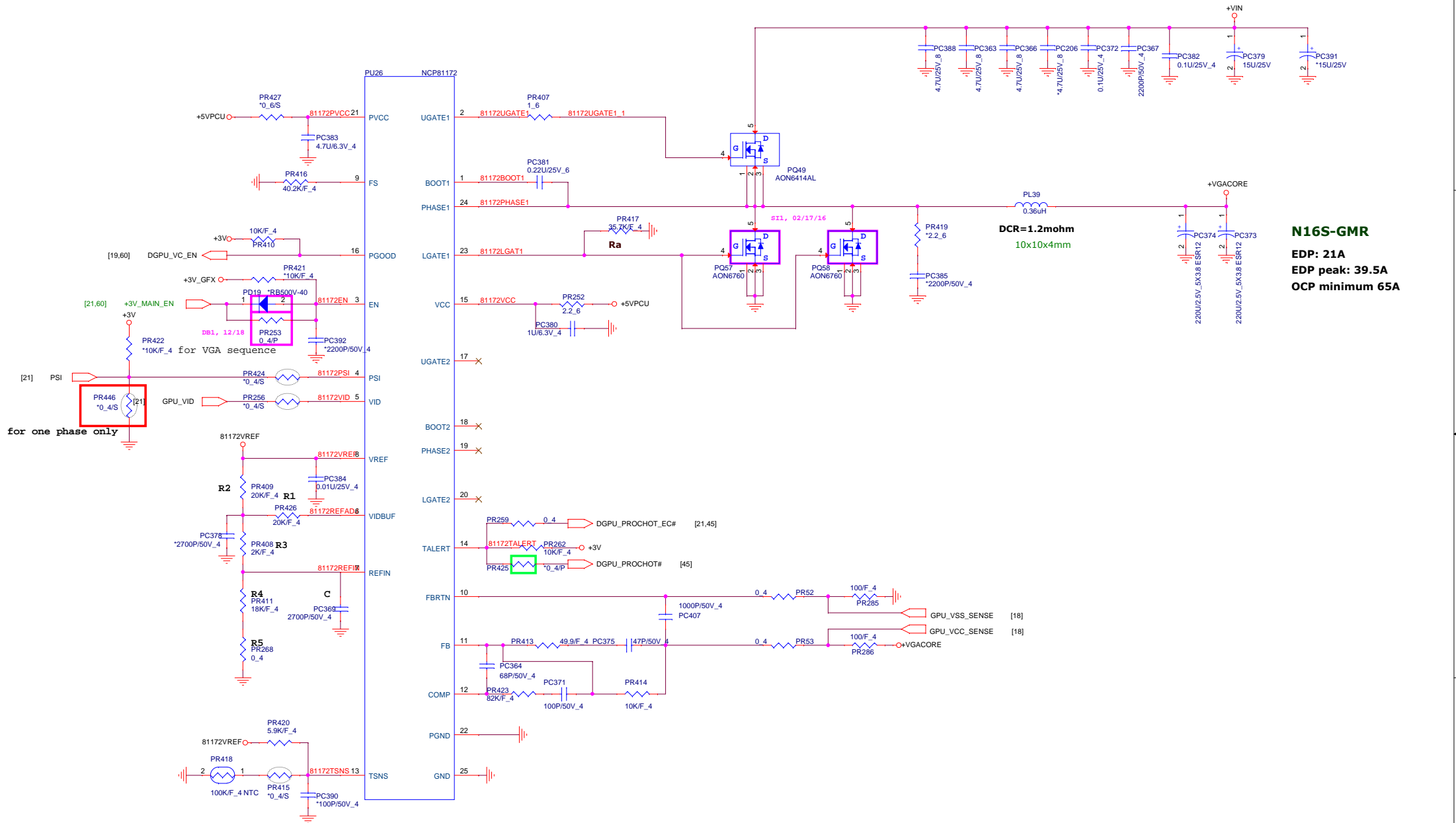


PROJECT:400 Series
Quanta Computer Inc.

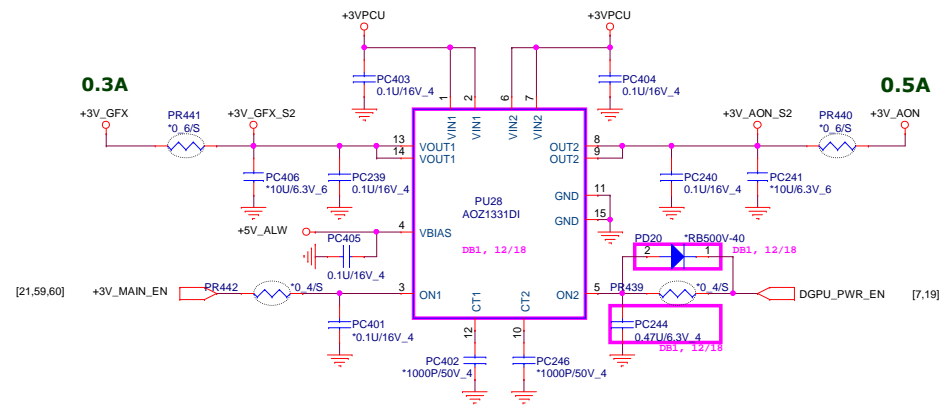
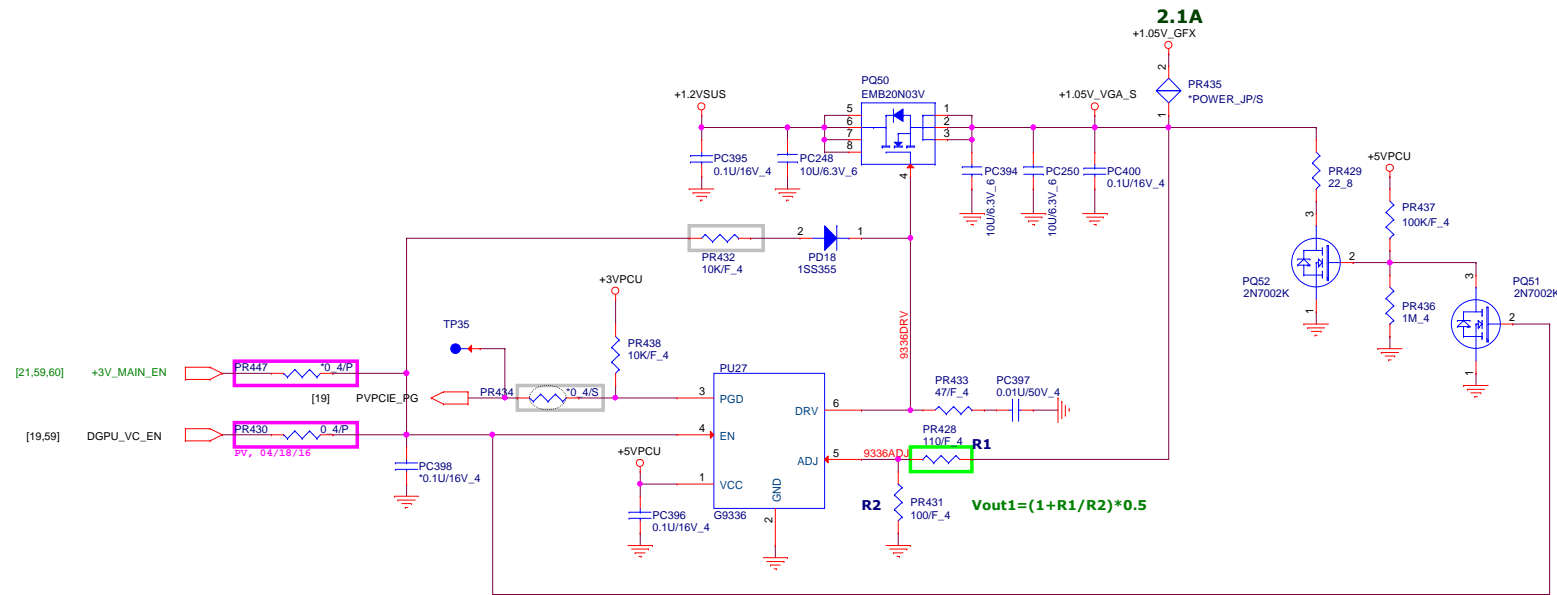
Size Custom	Document Number 55 - CPU VR IC (NCP81206)	Rev 1A
Date: Thursday, May 12, 2016	Sheet 56 of 65	

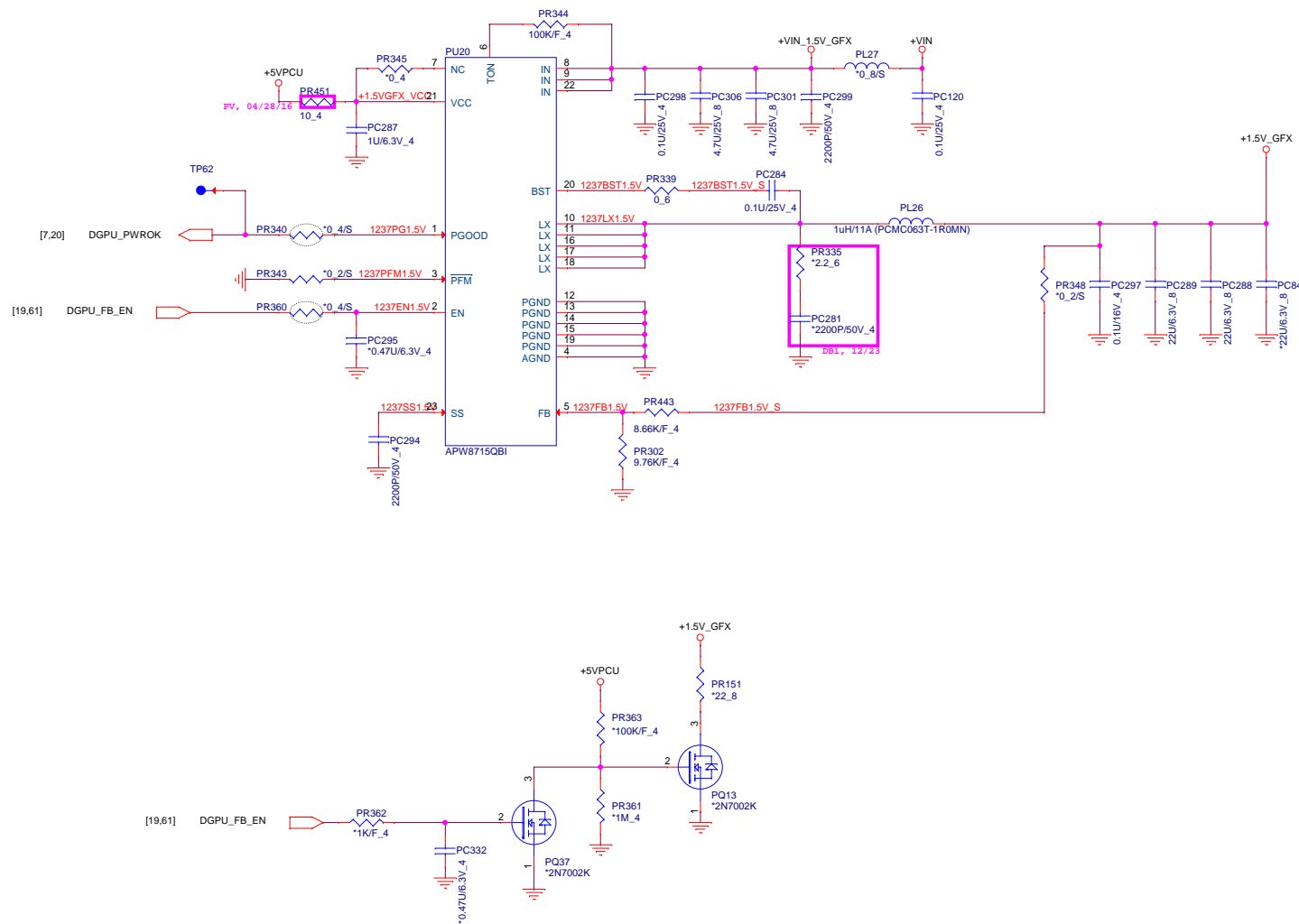







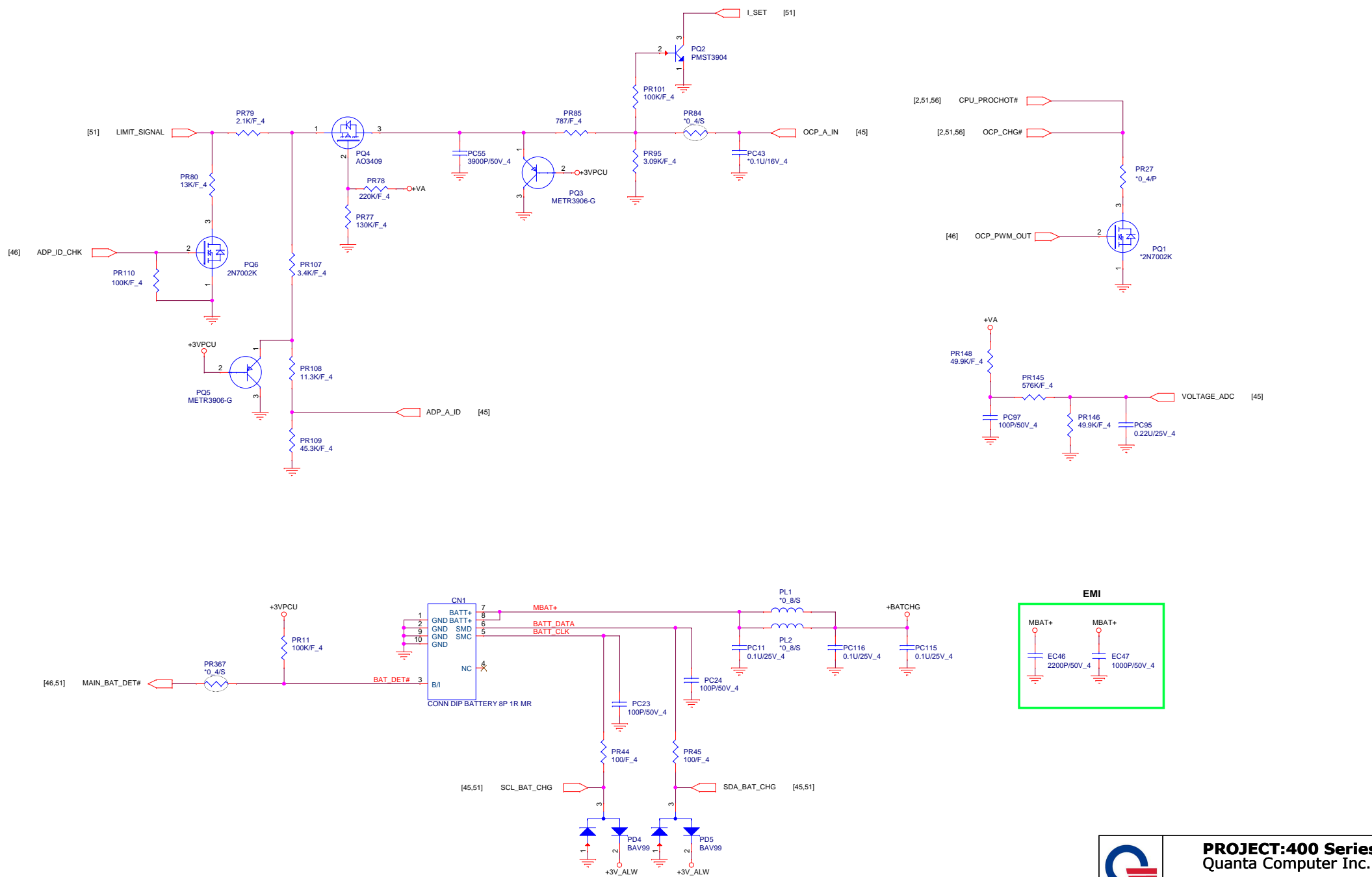
N16S-GMR
EDP: 21A
EDP peak: 39.5A
OCP minimum 65A






 NB5	PROJECT:400 Series		
	Quanta Computer Inc.		
	Size Custom	Document Number 61 -- +1.35V_GFX (AO21267)	Rev 1A
	Date: Thursday, May 12, 2016	Sheet	61 of 65

Adapter OCP





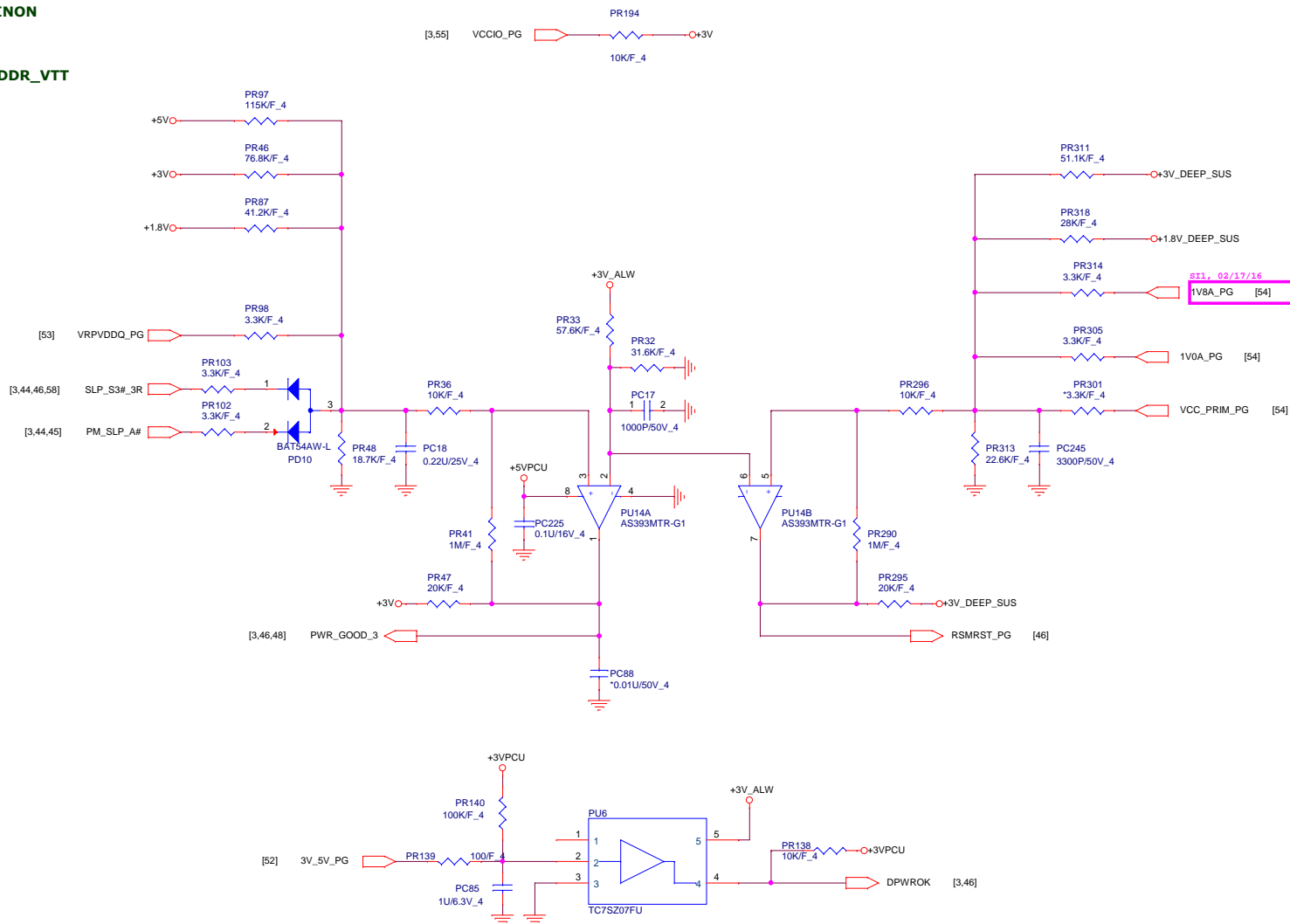
PROJECT:400 Series
Quanta Computer Inc.

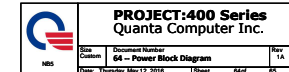
Size	Document Number	Rev
	62 - CHARGER II	1A
Date:	Thursday, May 12, 2016	Sheet 62 of 65

I'm from VIETNAM sualaptop365

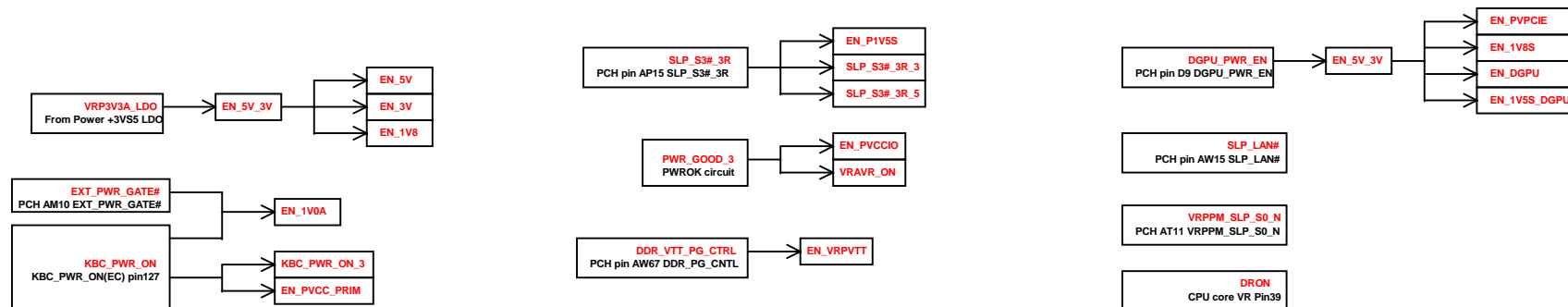
POK CKT

```
PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S = +0.75V_DDR_VTT
```



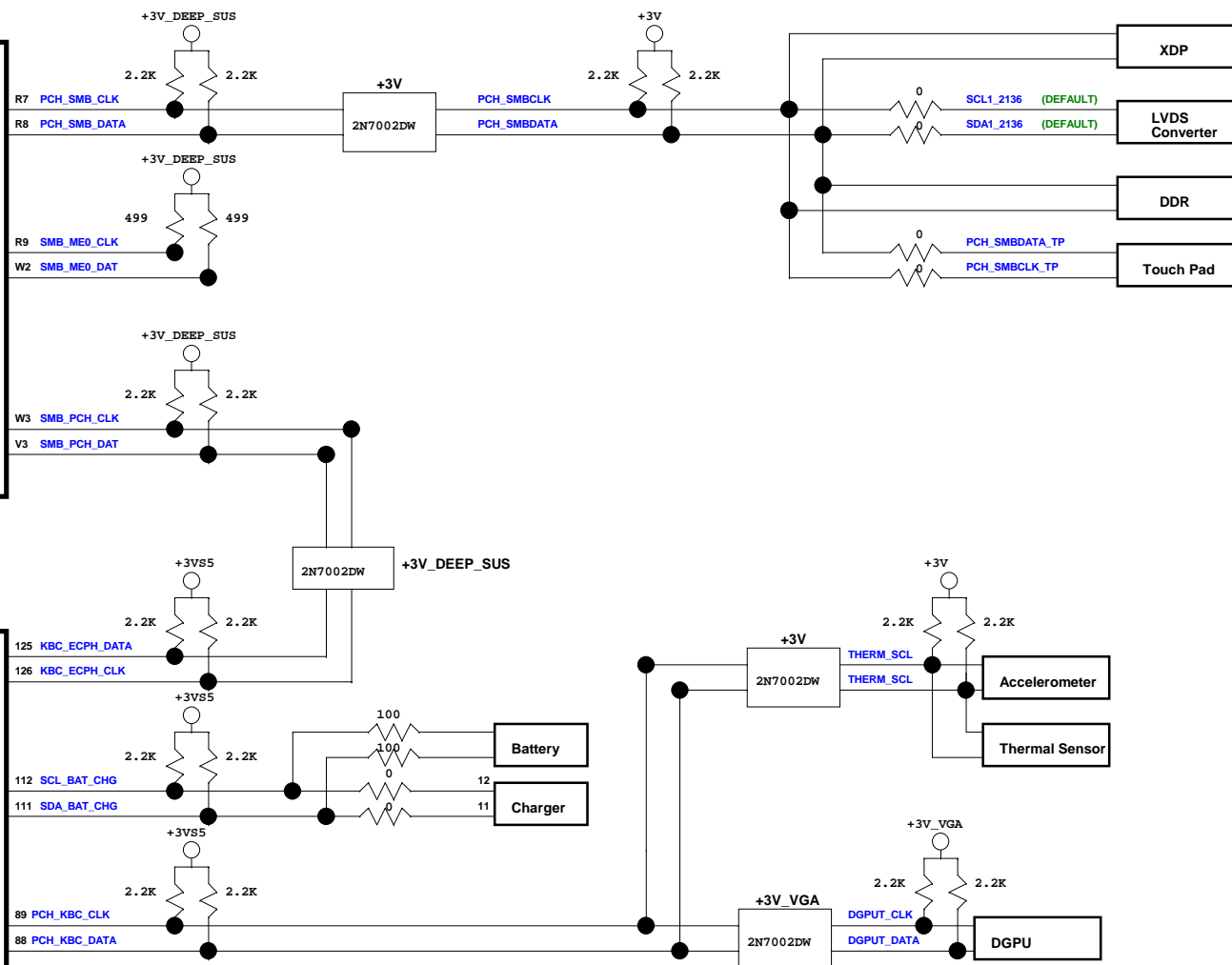


I'm from VIETNAM_sualaptop365



SKYLAKE U

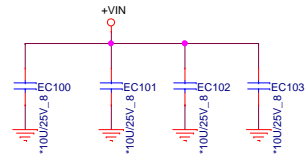
EC
NPCE586H




Example: *499/F_4 and *0_6/S
 * means none-installed
 499 means value
 F means 1%
 _4 means 0402 size
 /S means short pad

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC



 NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size Custom	Document Number 66 -- EMI and ISN	Rev 1A
	Date: Thursday, May 12, 2016 Sheet 66 of 66		